UNIT I

SEMICONDUCTOR DIODE

SEMICONDUCTOR

A **semiconductor** is a material which has electrical conductivity to a degree between that of a metal (such as copper) and that of an insulator (such as glass). Semiconductors are the foundation of modern electronics, including transistors, solar cells, light-emitting diodes (LEDs), quantum dots and digital and analog integrated circuits.

DIODE

Diode – Di + ode

Di means two and ode means electrode. So physical contact of two electrodes is known as diode and its important function is alternative current to direct current.

REVIEW OF INTRINSIC AND EXTRINSIC SEMICONDUCTORS

INTRINSIC SEMICONDUCTOR

An intrinsic semiconductor is one, which is pure enough that impurities do not appreciably affect its electrical behavior. In this case, all carriers are created due to thermally or optically excited electrons from the full valence band into the empty conduction band.

Thus equal numbers of electrons and holes are present in an intrinsic semiconductor. Electrons and holes flow in opposite directions in an electric field, though they contribute to current in the same direction since they are oppositely charged. Hole current and electron current are not necessarily equal in an intrinsic semiconductor, however, because electrons and holes have different effective masses (crystalline analogues to free inertial masses).

The concentration of carriers is strongly dependent on the temperature. At low temperatures, the valence band is completely full making the material an insulator.

Both silicon and germanium are tetravalent, i.e. each has four electrons (valence electrons) in their outermost shell. Both elements crystallize with a diamond-like structure, i.e. in such a way that each atom in the crystal is inside a tetrahedron formed by the four atoms which are closest to it. Each atom shares its four valence electrons with its four immediate neighbours, so that each atom is involved in four covalent bonds.

EXTRINSIC SEMICONDUCTOR

An extrinsic semiconductor is one that has been doped with impurities to modify the number and type of free charge carriers. An extrinsic semiconductor is a semiconductor that has been *doped*, that is, into which a doping agent has been introduced, giving it different electrical properties than the intrinsic (pure) semiconductor.

Doping involves adding dopant atoms to an intrinsic semiconductor, which changes the electron and hole carrier concentrations of the semiconductor at thermal equilibrium. Dominant carrier concentrations in an extrinsic semiconductor classify it as either an n-type or p-type semiconductor. The electrical properties of extrinsic semiconductors make them essential components of many electronic devices.

A pure or intrinsic conductor has thermally generated holes and electrons. However these are relatively few in number. An enormous increase in the number of charge carriers can by achieved by introducing impurities into the semiconductor in a controlled manner.

The result is the formation of an extrinsic semiconductor. This process is referred to as doping. There are basically two types of impurities: donor impurities and acceptor impurities. Donor impurities are made up of atoms (arsenic for example) which have five valence electrons. Acceptor impurities are made up of atoms (gallium for example) which have three valence electrons.

The two types of extrinsic semiconductor

N-TYPE SEMICONDUCTORS

Extrinsic semiconductors with a larger electron concentration than hole concentration are known as n-type semiconductors. The phrase 'n-type' comes from the negative charge of the electron. In n-type semiconductors, electrons are the majority carriers and holes are the minority carriers. N-type semiconductors are created by doping an intrinsic semiconductor with donor.

impurities. In an n-type semiconductor, the Fermi energy level is greater than that of the intrinsic semiconductor and lies closer to the conduction band than the valence band. Arsenic has 5 valence electrons, however, only 4 of them form part of covalent bonds. The 5th electron is then free to take part in conduction. The electrons are said to be the majority carriers and the holes are said to be the minority carriers.

P-TYPE SEMICONDUCTORS

As opposed to n-type semiconductors, p-type semiconductors have a larger hole concentration than electron concentration. The phrase 'p-type' refers to the positive charge of the hole. In p-type semiconductors, holes are the majority carriers and electrons are the minority carriers. P-type semiconductors are created by doping an intrinsic semiconductor with acceptor impurities. P-type semiconductors have Fermi energy levels below the intrinsic Fermi energy level.

The Fermi energy level lies closer to the valence band than the conduction band in a p-type semiconductor. Gallium has 3 valence electrons, however, there are 4 covalent bonds to fill. The 4^{th} bond therefore remains vacant producing a hole. The holes are said to be the majority carriers and the electrons are said to be the minority carriers.

PN JUNCTION :

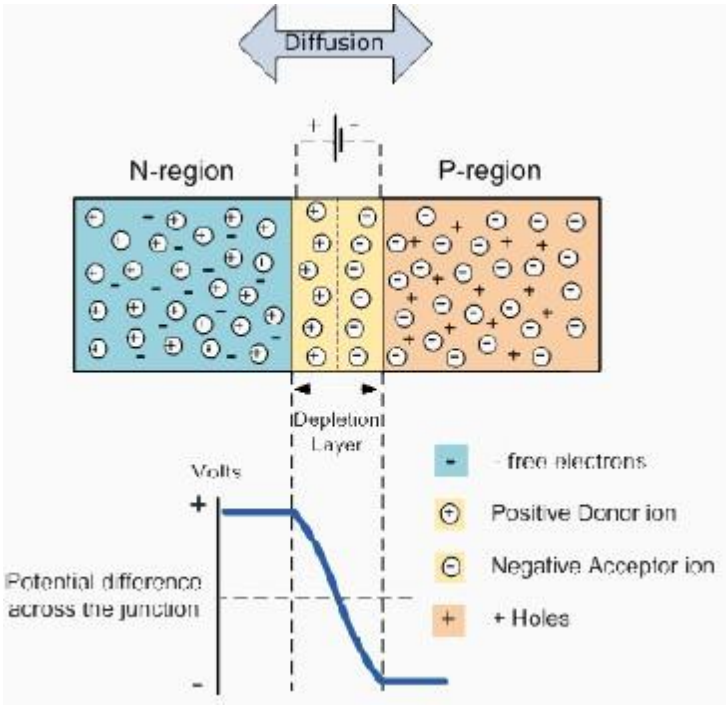
When the N and P-type semiconductor materials are first joined together a very large density gradient exists between both sides of the junction so some of the free electrons from the donor impurity atoms begin to migrate across this newly formed junction to fill up the holes in the P-type material producing negative ions.

However, because the electrons have moved across the junction from the N-type silicon to the P-type silicon, they leave behind positively charged donor ions (ND) on the negative side and now the holes from the acceptor impurity migrate across the junction in the opposite direction into the region are there are large numbers of free electrons. As a result, the charge density of the P-type along the junction is filled with negatively charged acceptor ions (NA), and the charge density of the N-type along the junction becomes positive. This charge transfer of electrons and holes across the junction is known as diffusion.

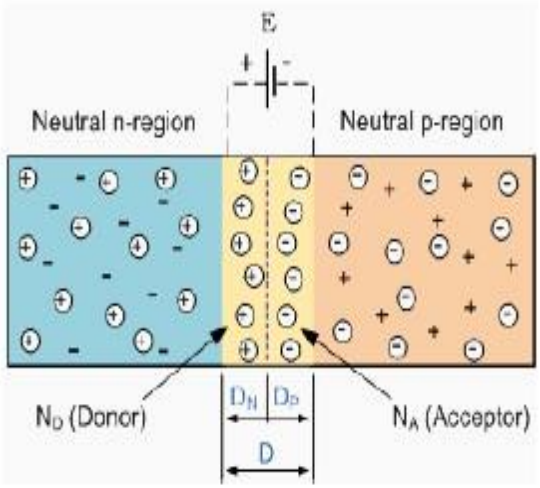
This process continues back and forth until the number of electrons which have crossed the junction have a large enough electrical charge to repel or prevent any more carriers from crossing the junction. The regions on both sides of the junction become depleted of any free carriers in comparison to the N and P type materials away from the junction. Eventually a state of equilibrium (electrically neutral situation) will occur producing a "potential barrier" zone around the area of the junction as the donor atoms repel the holes and the acceptor atoms repel the electrons. Since no free charge carriers can rest in a position where there is a potential barrier the regions on both sides of the junction become depleted of any more free carriers in comparison to the N and P type materials away from the junction. This area around the junction is now called the Depletion Layer.

THE PN JUNCTION

The total charge on each side of the junction must be equal and opposite to maintain a neutral charge condition around the junction. If the depletion layer region has a distance D, it therefore must therefore penetrate into the silicon by a distance of Dp for the positive side, and a distance of Dn for the negative side giving a relationship between the two of Dp.NA = Dn.ND in order to maintain charge neutrality also called equilibrium.



PN JUNCTION DIODE:



As the N-type material has lost electrons and the P-type has lost holes, the N-type material has become positive with respect to the P-type.

Then the presence of impurity ions on both sides of the junction cause an electric field to be established across this region with the N- side at a positive voltage relative to the P-side. The problem now is that a free charge requires some extra energy to overcome the barrier that now exists for it to be able to cross the depletion region junction. This electric field created by the diffusion process has created a "built-in potential difference" across the junction with an open-circuit (zero bias) potential of:

$$E_o = V_T \ln\left(\frac{N_D . N_A}{n_i^2}\right)$$

Where: Eo is the zero bias junction voltage, VT the thermal voltage of 26mV at room temperature, ND and NA are the impurity concentrations and ni is the intrinsic concentration.

A suitable positive voltage (forward bias) applied between the two ends of the PN junction can the free electrons and holes with the extra energy. The external voltage required to overcome this potential barrier that now exists is very much dependent upon the type of semiconductor material used and its actual temperature.

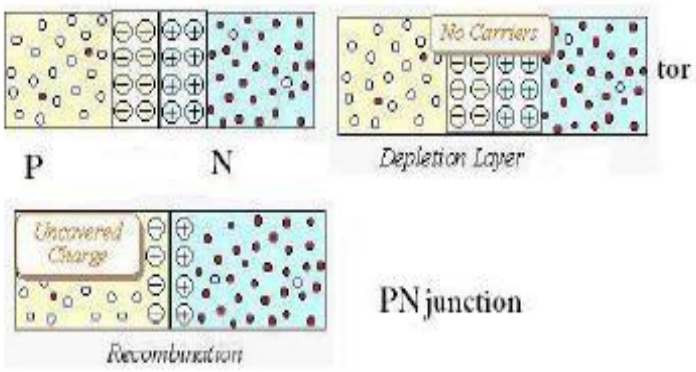
Typically at room temperature the voltage across the depletion layer for silicon is about 0.6 - 0.7 volts and for germanium is about
0.3 - 0.35 volts. This potential barrier will always exist even if the device is not connected to any external power source.

The significance of this built-in potential across the junction, is that it opposes both the flow of holes and electrons across the junction and is why it is called the potential barrier. In practice, a PN junction is formed within a single crystal of material rather than just simply joining or fusing together two separate pieces.

Electrical contacts are also fused onto either side of the crystal to enable an electrical connection to be made to an external circuit. Then the resulting device that has been made is called a PN junction Diode or Signal Diode.

DEPLETION LAYER PN JUNCTION

If one side of crystal pure semiconductor Si(silicon) or Ge(Germanium) is doped with acceptor impurity atoms and the other side is doped with donor impurity atoms , a PN junction is formed as shown in figure.P region has high concentration of holes and N region contains large number of electrons.



As soon as the junction is formed, free electrons and holes cross through the junction by the process of diffusion. During this process , the electrons crossing the junction from N- region into P-region , recombine with holes in the P-region very close to the junction. Similarly holes crossing the junction from the P-region into the N-region, recombine with electrons in the N-region very close to the junction. Thus a region is formed, which does not have any mobile charge very close to the junction. This region is called the depletion layer of pn junction.

In this region, on the left side of the junction, the acceptor atoms become negative ions and on the right side of the junction, the donor atoms become positive ions as shown in figure.

FUNCTION OF DEPLETION LAYER OF PN JUNCTION

An electric field is set up, between the donor and acceptor ions in the depletion layer of the pn junction .The potential at the N-side is higher than the potential at P-side. Therefore electrons in the N- side are prevented to go to the lower potential of P-side. Similarly, holes in the P-side find themselves at a lower potential and are prevented to cross to the N-side. Thus, there is a barrier at the junction which opposes the movement of the majority charge carriers. The difference of potential from one side of the barrier to the other side of the barrier is called potential barrier. The potential barrier is approximately 0.7V for a silicon PN junction and 0.3V for germanium PN junction. The distance from one side of the barrier to the other side is called the width of the barrier, which depends on the nature of the material.

CURRENT EQUATION:

To derive the expression for the total current as function of applied voltage (neglect the barrier width)

When diode is forward biased, holes injected from the p to n material. The concentration p_n of holes in the n-side is increased above equilibrium value p_{no}

$$I = I_o\,[e^{(V/\eta V_T)} - 1]$$

where

I – diode current

I_o – diode reverse saturation current at room temperature

V – external voltage applied to the diode

Ƞ - a constant, 1 for Ge and 2 for Si

$V_T = kT/q = T/11600$, thermal voltage

K – Boltzmann's constant (1.38066x10^-23 J/K)

q – charge of electron (1.6x10^-19 C)

T – temperature of the diode junction

At room temperature (T=300 K), V_T = 26mV. Substituting this value in current equation,

$$I = I_o[e^{(40\,V/\eta)} - 1]$$

For germanium diode,

$$I = I_o\,[e^{40V} - 1]$$ since Ƞ =1 for Ge

For silicon diode,

since Ƞ =2 for Si. $$I = I_o[e^{20V} - 1]$$

If the value of applied voltage is greater than unity, then the equation of diode current for germanium,

$$I = I_o\,(e^{40V})$$

and for silicon,

$$I = I_o\,(e^{20V})$$

when the diode is reverse biased, its current equation may be obtained by changing the sign of voltage V. Thus diode current with reverse bias is

$$I = I_o\,[e^{(-V/\eta V_T)} - 1]$$

If $V >> V_T$ then the term $e^{(-V/\eta VT)} << 1$ therefore I=Io termed as reverse saturation current, which is valid as long as the external voltage is below the breakdown value.

DRIFT AND DIFFUSION CURRENTS

→ The flow of charge (ie) current through a semiconductor material are of two types namely drift & diffusion.

→ (ie) The net current that flows through a (PN junction diode) semiconductor material has two components

(i) Drift current
(ii) Diffusion current

DRIFT CURRENT

→ When an electric field is applied across the semiconductor material, the charge carriers attain a certain drift velocity V_d , which is equal to the product of the mobility of the charge carriers and the applied Electric Field intensity E ;

Drift velocity V_d = mobility of the charge carriers X Applied Electric field intensity.

→ Holes move towards the negative terminal of the battery and electrons move towards the positive terminal of the battery. This combined effect of movement of the charge carriers constitutes a current known as — the drift current — .

→ Thus the drift current is defined as the flow of electric current due to the motion of the charge carriers under the influence of an external electric field.

→ Drift current due to the charge carriers such as free electrons and holes are the current passing through a square centimeter perpendicular to the direction of flow.

(i) Drift current density J_n , due to free electrons is given by
$$J_n = q\, n\, \mu_n\, E \ A / cm^2$$

(ii) Drift current density J_P, due to holes is given by
$$J_P = q\, p\, \mu_p\, E \ A / cm^2$$

Where, n - Number of free electrons per cubic centimeter.

P - Number of holes per cubic centimeter

μ_n – Mobility of electrons in cm^2 / Vs

μ_p – Mobility of holes in cm^2 / Vs

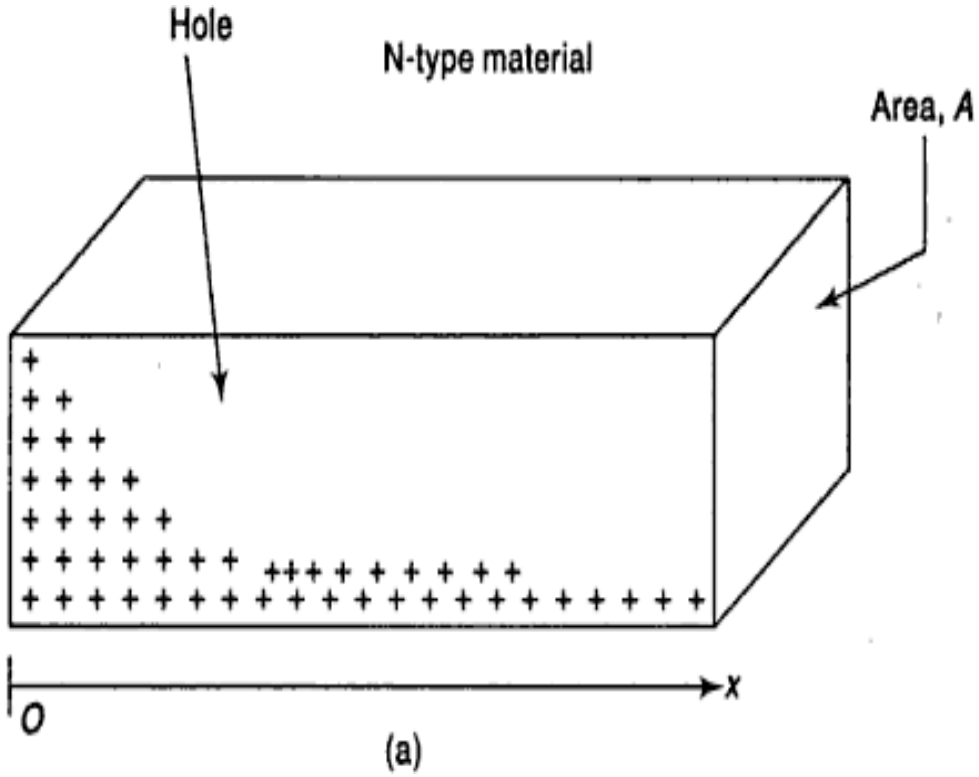
E – Applied Electric filed Intensity in V /cm

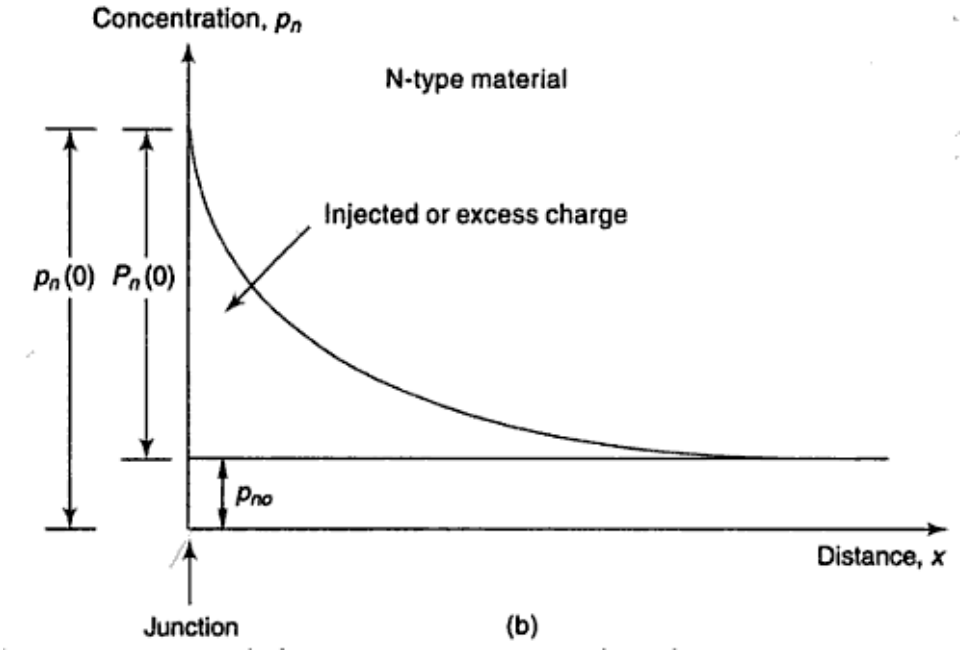
q – Charge of an electron = 1.6×10^{-19} coulomb.

DIFFUSION CURRENT

→ It is possible for an electric current to flow in a semiconductor even in the absence of the applied voltage provided a concentration gradient exists in the material.

→ A concentration gradient exists if the number of either elements or holes is greater in one region of a semiconductor as compared to the rest of the Region.





(a) Exess hole concentration varying along the axis in an N-type semiconductor bar
(b) The resulting diffusion current

→ In a semiconductor material the change carriers have the tendency to move from the region of higher concentration to that of lower concentration of the same type of charge carriers. Thus the movement of charge carriers takes place resulting in a current called diffusion current.

As indicated in fig a, the hole concentration p(x) in semiconductor bar varies from a high value to a low value along the x-axis and is constant in the y and z directions.

Diffusion current density due to holes J_p is given by

$$J_p = -qD_p \frac{dp}{dx} \text{ A/cm}^2$$

Since the hole density p(x) decreases with increasing x as shown in fig b, dp/dx is negative and the minus sign in equation is needed in order that J_p has positive sign in the positive x direction.

Diffusion current density due to the free electrons is given by

$$J_n = qD_n \frac{dn}{dx} \text{ A/cm}^2$$

Where dn/dx – concentration gradient for electrons

Dp/dx - concentration gradient for holes

D_n and D_p – diffusion coefficient for electrons and holes

Total Current

The total current in a semiconductor is the sum of both drift and diffusion currents that is given by

$$J_p = qp\mu_p E - qD_p \frac{dp}{dx}$$

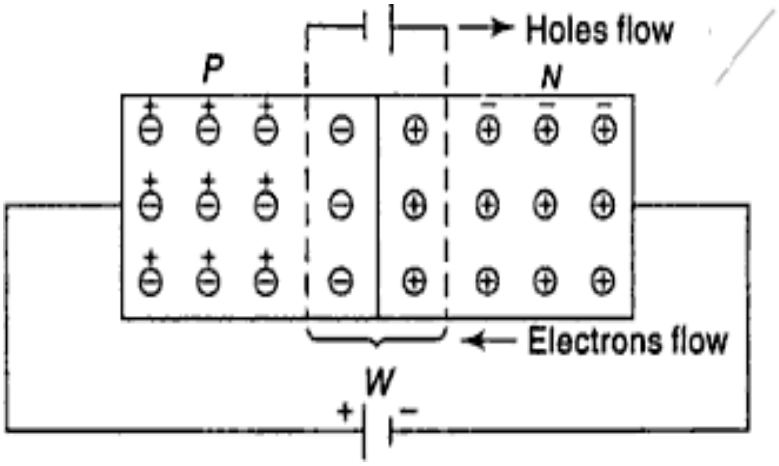
Similarly the total current density for an N type semiconductor is given by

$$J_n = qn\ \mu_n\ E + qD_n \frac{dn}{dx}$$

FORWARD BIAS CONDITION

When positive terminal of the battery is connected to the P-type and negative terminal to N-type of the PN junction diode that is known as forward bias condition.

Operation



The applied potential in external battery acts in opposition to the internal potential barrier which disturbs the equilibrium.

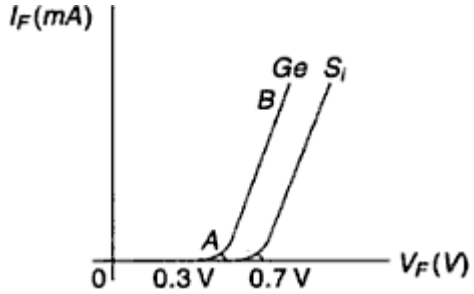
As soon as equilibrium is disturbed by the application of an external voltage, the Fermi level is no longer continuous across the junction.

Under the forward bias condition the applied positive potential repels the holes in P type region so that the holes move towards the junction and the applied positive potential repels the electrons in N type region so that the electrons move towards the junction.

When the applied potential is more than the internal barrier potential the depletion region and internal potential barrier disappear.

V-I Characteristics

As the forward voltage increased for $V_F < Vo$, the forward current I_F almost zero because the potential barrier prevents the holes from P region and electrons from N region to flow across the depletion region in opposite direction.



For $V_F > Vo$, the potential barrier at the junction completely disappears and hence, the holes cross the junction from P to N type and electrons cross the junction to opposite direction, resulting large current flow in external circuit.

A feature noted here is the cut in voltage or threshold voltage V_F below which the current is very small.

At this voltage the potential barrier is overcome and the current through the junction starts to increase rapidly.

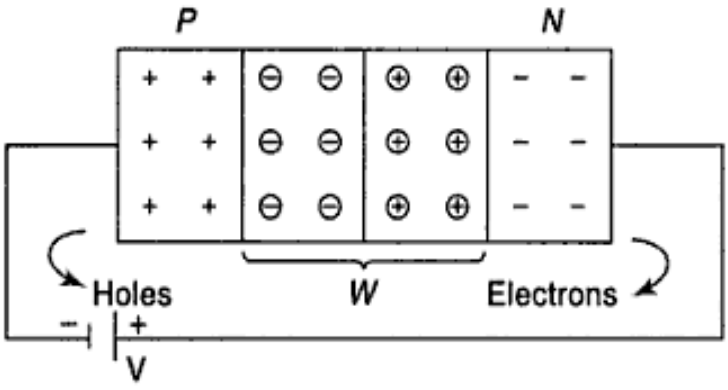
Cut in voltage is 0.3V for germanium and 0.7 for silicon.

UNDER REVERSE BIAS CONDITION

When the negative terminal of the battery is connected to the P-type and positive terminal to N-type of the PN junction diode that is known as forward bias condition.

Operation

The holes from the majority carriers of the P side move towards the negative terminal of the battery and electrons which from the majority carrier of the N side are attracted towards the positive terminal of the battery.

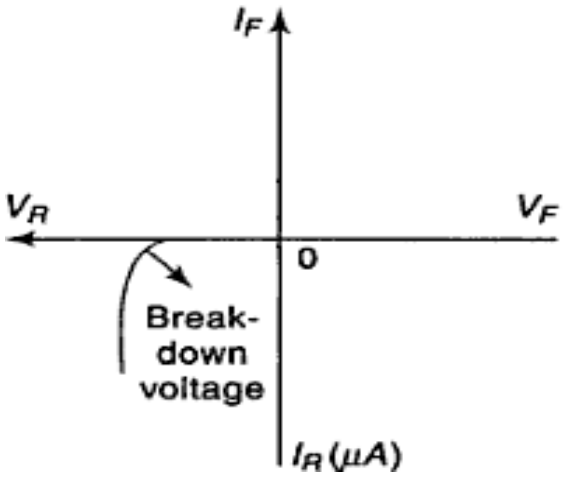


Hence, the width of the depletion region which is depleted of mobile charge carriers increases. Thus, the electric field produced by applied reverse bias, is in the same direction as the electric field of the potential barrier.

Hence the resultant potential barrier is increased which prevents the flow of majority carriers in both directions. The depletion width W is proportional to under reverse bias.

V-I characteristics

Theoretically no current flow in the external circuit. But in practice a very small amount of current of the order of few microamperes flows under reverse bias.



Electrons forming covalent bonds of semiconductor atoms in the P and N type regions may absorb sufficient energy from heat and light to cause breaking covalent bonds. So electron hole pairs continuously produced.

Consequently the minority carriers electrons in the P region and holes in the N region, wander over to the junction and flow towards their majority carrier side giving rise a small reverse current. This current is known as **reverse saturation current Io**.

The magnitude of this current is depends on the temperature because minority carrier is thermally broken covalent bonds.

TRANSITION AND DIFFUSION CAPACITANCES:

1. Maximum Forward Current

The Maximum Forward Current (IF(max)) is as its name implies the maximum forward current allowed to flow through the device. When the diode is conducting in the forward bias condition, it has a very small "ON" resistance across the PN junction and therefore, power is dissipated across this junction (Ohm´s Law) in the form of heat.

Then, exceeding its (IF(max)) value will cause more heat to be generated across the junction and the diode will fail due to thermal overload, usually with destructive consequences. When operating diodes around their maximum current ratings it is always best to provide additional cooling to dissipate the heat produced by the diode.

For example, our small 1N4148 signal diode has a maximum current rating of about 150mA with a power dissipation of 500mW at 25oC. Then a resistor must be used in series with the diode to limit the forward current, (IF(max)) through it to below this value.

2. Peak Inverse Voltage

The Peak Inverse Voltage (PIV) or Maximum Reverse Voltage (VR(max)), is the maximum allowable Reverse operating voltage that can be applied across the diode without reverse breakdown and damage occurring to the device. This rating therefore, is usually less than the "avalanche breakdown" level on the reverse bias characteristic curve. Typical values of VR(max) range from a few volts to thousands of volts and must be considered when replacing a diode.

The peak inverse voltage is an important parameter and is mainly used for rectifying diodes in AC rectifier circuits with reference to the amplitude of the voltage were the sinusoidal waveform changes from a positive to a negative value on each and every cycle.

3. Forward Power Dissipation

Signal diodes have a Forward Power Dissipation, (PD(max)) rating. This rating is the maximum possible power dissipation of the diode when it is forward biased (conducting). When current flows through the signal diode the biasing of the PN junction is not perfect and offers some resistance to the flow of current resulting in power being dissipated (lost) in the diode in the form of heat.

As small signal diodes are nonlinear devices the resistance of the PN junction is not constant, it is a dynamic property then we cannot use Ohms Law to define the power in terms of current and resistance or voltage and resistance as we can for resistors. Then to find the power that will be dissipated by the diode we must multiply the voltage drop across it times the current flowing through it: PD = VxI

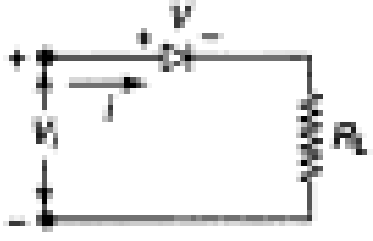
4. Maximum Operating Temperature

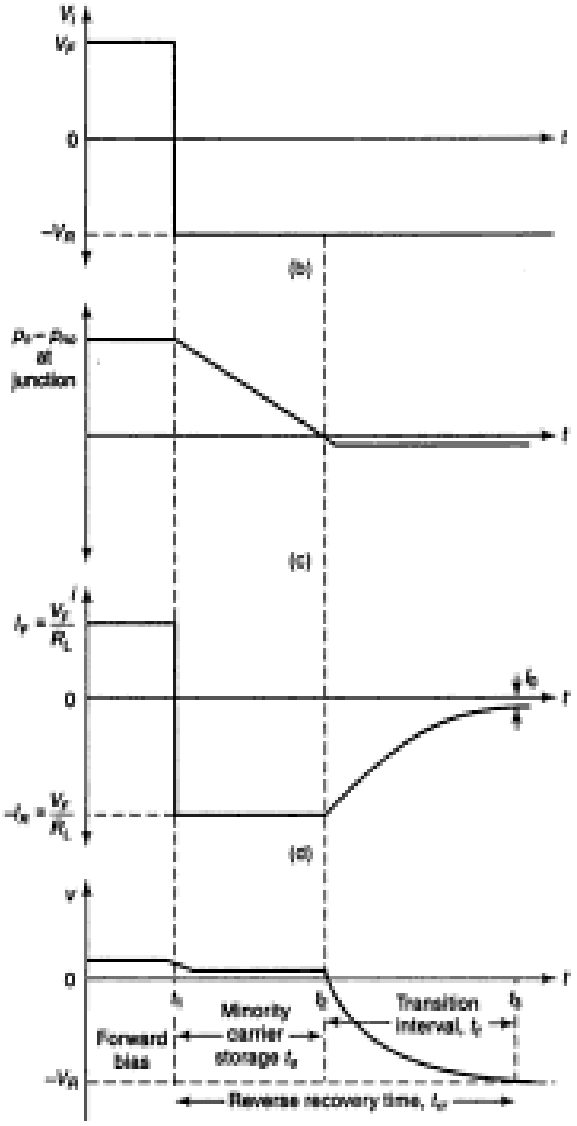
The Maximum Operating Temperature actually relates to the Junction Temperature (TJ) of the diode and is related to maximum power dissipation. It is the maximum temperature allowable before the structure of the diode deteriorates and is expressed in units of degrees centigrade per Watt, (oC/W). This value is linked closely to the maximum forward current of the device so that at this value the temperature of the junction is not exceeded. However, the maximum forward current will also depend upon the ambient temperature in which the device is operating so the maximum forward current is usually quoted for two or more ambient temperature values such as 25oC or 70oC.

SWITCHING CHARACTERISTICS

Diodes are often used in switching mode. When the applied bias voltage to the PN diode is suddenly reversed in opposite direction and it reaches a steady state at a interval of time that is called the **recovery time**. Forward recovery time is defined is the time required the forward voltage or current to reach a specified value after switching diode from its reverse to forward biased state.

When PN diode is forward biased the minority electrons concentration in P region is linear. If the junction is suddenly reversed at t1 then because of stored electronic charge, the reverse current I_R is initially of the same magnitude as forward current I_F.





The diode will continue to conduct until the injected or excess minority carrier density (p-po) or (n-no) has dropped to zero shown in fig. c.

In fig. b the applied voltage Vi = V_F for the time up to t1 is in the direction to forward bias the diode. The resistance R_L is large so that the drop across R_L is large when compared to the drop across diode. Then the current is I= V_F / R_L = I

At time t=t1 the input voltage is reversed to the value of –V_R current does not become zero and the value is I= V_R / R_L = I_R shown in fig d..

During the time interval from t1 to t2 the injected minority carriers have remained stored and hence this interval is called the **storage time (t1).**

After the instant t=t2, the diode gradually recovers and ultimately reaches the steady state. The time interval between t2 and instant t3 when the diode has recovered nominally is called the **transition time t_t**.

The recovery said to have completed (i) when even the minority carriers remote from the junction have difference to the junction and crossed it. (ii) when the junction transition capacitance C across the reverse biased junction has got charged through the external resistor R_L to the voltage $-V_R$.

For commercial switching type diodes the reverse recovery time t_{rr} ranges from less than 1ns up to as high as 1us.

In order to minimize the effect of reverse current the time period of the operating frequency should be a minimum of approximately 10 times t_{rr}. For example if diode has t_{rr} of 2ns its operating frequency is

$$f_{max} = \frac{1}{T} = \frac{1}{10 \times t_{rr}} = \frac{1}{10 \times 2 \times 10^{-9}} = 50 \text{ MHz}$$

The reverse recovery time can be reduced b shortening the length of the P region in a PN junction diode.

The stored storage and switching time can be reduced by introduction of gold impurities into junction diode by diffusion. The gold dopant also called a **life time killer**, increases the recombination rate and removes the stored minority carriers.

This technique is used to produce diodes and other active devices for high speed applications.

APPLICATION OF PN DIODE

- Can be used as rectifier in DC Power Supplies.
- In Demodulation or Detector Circuits.
- In clamping networks used as DC Restorers
- In clipping circuits used for waveform generation.
- As switches in digital logic circuits.
- In demodulation circuits

UNIT II

BIPOLAR JUNCTION TRANSISTORS

TRANSISTOR CHARACTERISTICS:

The basic of electronic system nowadays is semiconductor device.

The famous and commonly use of this device is BJTs

The transistor formed by back to back connection of two diodes.

Bipolar Junction Transistors : The operation of the transistor depends on both majority and minority carriers.

The voltage between two terminals controls the current through the third terminal. So it is called current controlled device.

It can be use as amplifier and logic switches.

BJT consists of three terminal:

- collector : C
- base : B
- emitter : E

Two types of BJT : pnp and npn

Transistor Construction

- 3 layer semiconductor device consisting:
    - 2 n- and 1 p-type layers of material - npn transistor
    - 2 p- and 1 n-type layers of material - pnp transistor
- The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material
- A single pn junction has two different types of bias:
    - forward bias
    - reverse bias
- Thus, a two-pn-junction device has four types of bias.

Position of the terminals and symbol of BJT.

- Base is located at the middle and more thin from the level of collector and emitter
- The emitter and collector terminals are made of the same type of semiconductor material, while the base of the other type of material

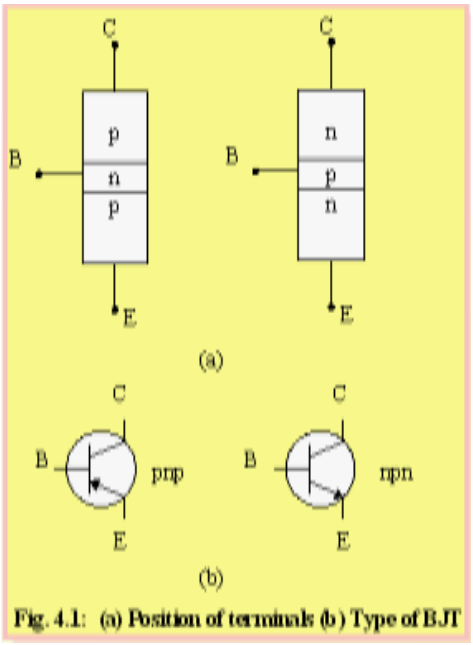
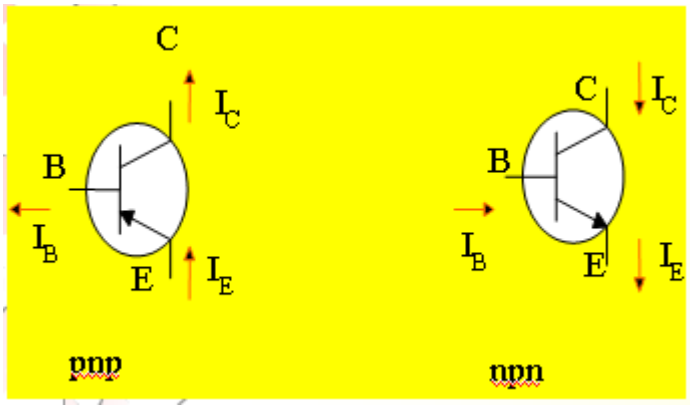


Fig. 4.1: (a) Position of terminals (b) Type of BJT

Transistor currents



- The arrow is always drawn on the emitter The arrow always point toward the n-type

- The arrow indicates the direction of the emitter current:

pnp:E-> B

npn: B-> E

I_C = the collector current

I_B = the base current

I_E = the emitter current

Transistor Operation

• The basic operation will be described using the pnp transistor. The operation of the pnp transistor is exactly the same if the roles played by the electron and hole are interchanged.

• One p-n junction of a transistor is reverse-biased, whereas the other is forward-biased

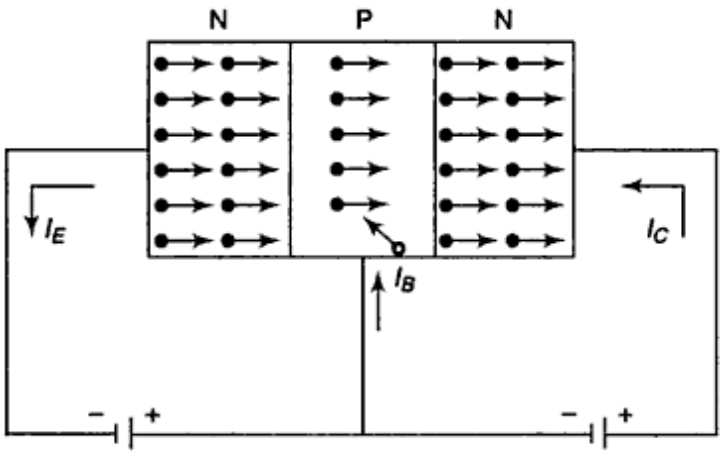


Fig. 6.4 Current in NPN transistor

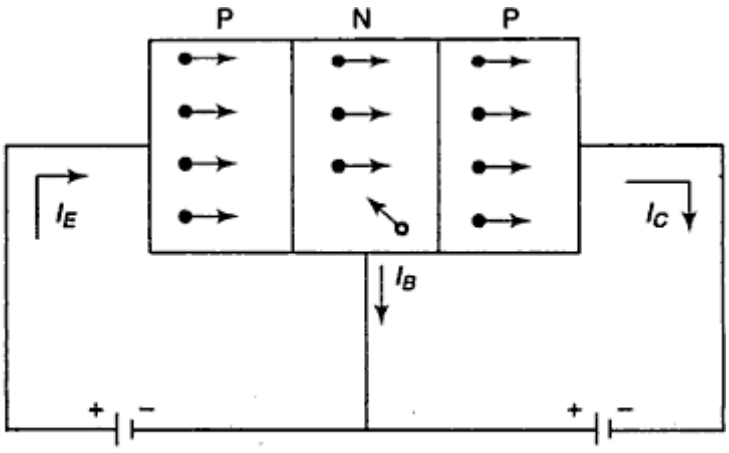


Fig. 6.5 Current in PNP transistor

• Both biasing potentials have been applied to a pnp transistor and resulting majority and minority carrier flows indicated.

• Majority carriers (+) will diffuse across the forward-biased p-n junction into the n-type material.

• A very small number of carriers (+) will through n-type material to the base terminal.

Resulting IB is typically in order of microamperes.

• The large number of majority carriers will diffuse across the reverse-biased junction into

the p-type material connected to the collector terminal.

• Majority carriers can cross the reverse-biased junction because the injected majority

carriers will appear as minority carriers in the n-type material.

• Applying KCL to the transistor :

$I_E = I_C + I_B$

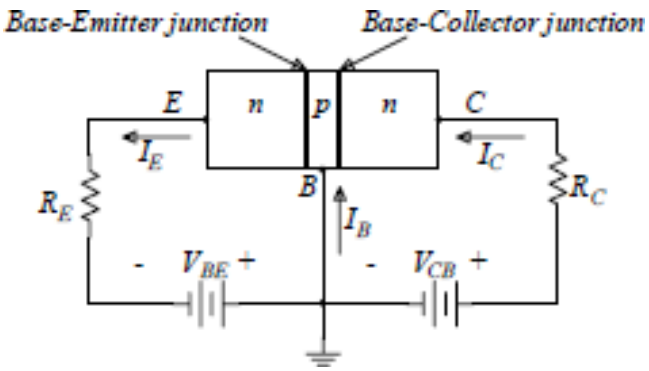
• The comprises of two components – the majority and minority carriers

$I_C = I_{Cmajority} + I_{COminority}$

• I_{CO} – I_C current with emitter terminal open and is called leakage current.

CURRENT EUATIONS

let‘s consider the BJT ***npn*** structure shown on Figure.



With the voltage V_{BE} and V_{CB} as shown, the Base-Emitter (B-E) junction is forward biased and the Base Collector (B-C) junction is reverse biased.

The current through the B-E junction is related to the B-E voltage as

$$I_E = I_s\left(e^{V_{BE}/V_T} - 1\right)$$

Due to the large differences in the doping concentrations of the emitter and the base regions the electrons injected into the base region (from the emitter region) results in the emitter current *EI*.

Furthermore the number of electrons injected into the collector region is directly related to the electrons injected into the base region from the emitter region.

Therefore, the collector current is related to the emitter current which is in turn a function of the B-E voltage.

The collector current and the base current are related by

$Ic = \beta I_B$

And by applying KCL we obtain

$I_E = Ic + I_B$

And thus from equations the relationship between the emitter and the base currents is

$I_E = (1+\beta)I_B$

And equivalently

$$Ic = (\beta / 1+\beta)I_E$$

The fraction $(\beta / 1+\beta)$ is called α,

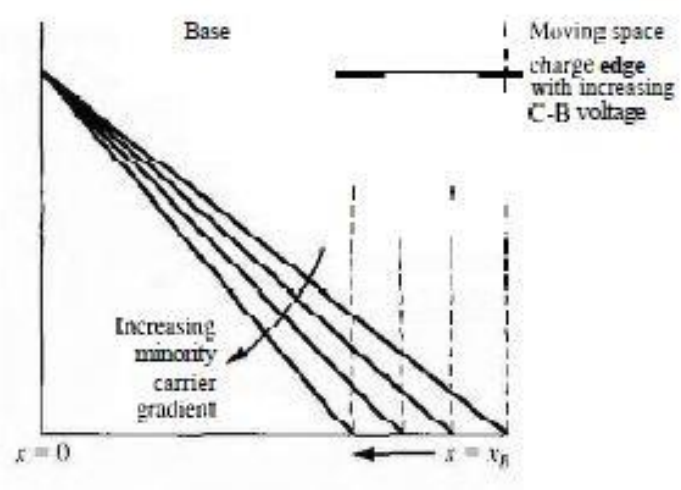
For the transistors of interest $\beta=100$ which corresponds to $\alpha= 0.99$ and $Ic = I_B$

The direction of the currents and the voltage polarities for the npn and the pnp BJTs are shown in fig.

Current directions and voltage polarities for *npn* (a) and *pnp* (b) BJTs

EARLY EFFECT (Base width modulation)

As the voltages applied to the base-emitter and base-collector junctions are changed, the depletion layer widths and the quasi-neutral regions vary as well. This causes the collector current to vary with the collector-emitter voltage as illustrated in Figure .



Variation of the minority-carrier distribution in the base quasi-neutral region due to a variation of the base-collector voltage.

A variation of the base-collector voltage results in a variation of the quasi-neutral width in the base. The gradient of the minority-carrier density in the base therefore changes, yielding an increased collector current as the collector-base current is increased. This effect is referred to as the Early effect.

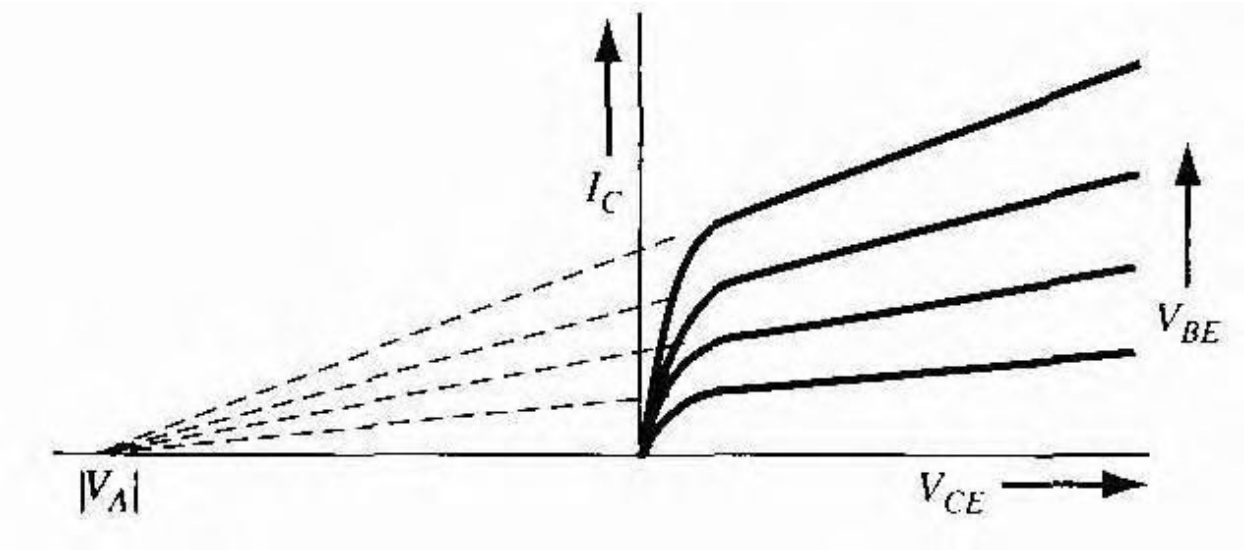
The Early effect is observed as an increase in the collector current with increasing collector-emitter voltage as illustrated with Figure. The Early voltage, V_A, is obtained by drawing a line tangential to the transistor *I-V* characteristic at the point of interest. The Early voltage equals the horizontal distance between the point chosen on the *I-V* characteristics and the intersection between the tangential line and the horizontal axis. It is indicated on the figure by the horizontal arrow.

The change of the collector current when changing the collector-emitter voltage is primarily due to the variation of the base-collector voltage, since the base-emitter junction is forward biased and a constant base current is applied. The collector current depends on the base-collector voltage since the base-collector depletion layer width varies, which also causes the quasi-neutral width, w_B', in the base to vary.

This variation can be calculated for a piece-wise uniformly-doped transistor using the ideal transistor mode.

(1)

$$\frac{dI_C}{dV_{CE}} \cong -\frac{dI_C}{dV_{BC}} = \frac{I_C}{w_B'}\frac{dw_B'}{dV_{BC}}$$



Collector current increase with an increase of the collector-emitter voltage due to the Early effect. The Early voltage, V_A, is also indicated on the figure.

This variation can be expressed by the Early voltage, V_A, which quantifies what voltage variation would result in zero collector current.

$$\frac{dI_C}{dV_{CE}} \triangleq \frac{I_C}{|V_A|} \tag{2}$$

It can be shown that the Early voltage also equals the majority carrier charge in the base, Q_B, divided by the base-collector junction capacitance, $C_{j,BC} = \varepsilon_s/(x_{p,BC} + x_{n,BC})$, where $x_{p,BC}$ and $x_{n,BC}$ are given by (6) .

$$|V_A| = \frac{Q_{p,B}}{C_{j,BC}} = \frac{qN_B w_B'}{\frac{\varepsilon_s}{x_{p,BC} + x_{n,BC}}} \tag{3}$$

The Early voltage can also be linked to the output conductance, r_0, which equals:

$$r_0 \triangleq \frac{dV_{CE}}{dI_C} = \frac{|V_A|}{I_C} \tag{4}$$

In addition to the Early effect, there is a less pronounced effect due to the variation of the base-emitter voltage, which changes the ideality factor of the collector current. However, the effect at the base-emitter junction is much smaller since the base-emitter junction capacitance is larger and the base-emitter voltage variation is very limited since the junction is forward biased. This effect does lead to a variation of the ideality factor, n, given by,

$$n = \frac{1}{V_t \dfrac{d \ln I_C}{dV_{BE}}} \cong 1 + \frac{V_t}{Q_{p,B}} C_{j,BE} = 1 + \frac{V_t}{|V_A|} \frac{C_{j,BE}}{C_{j,BC}} \tag{5}$$

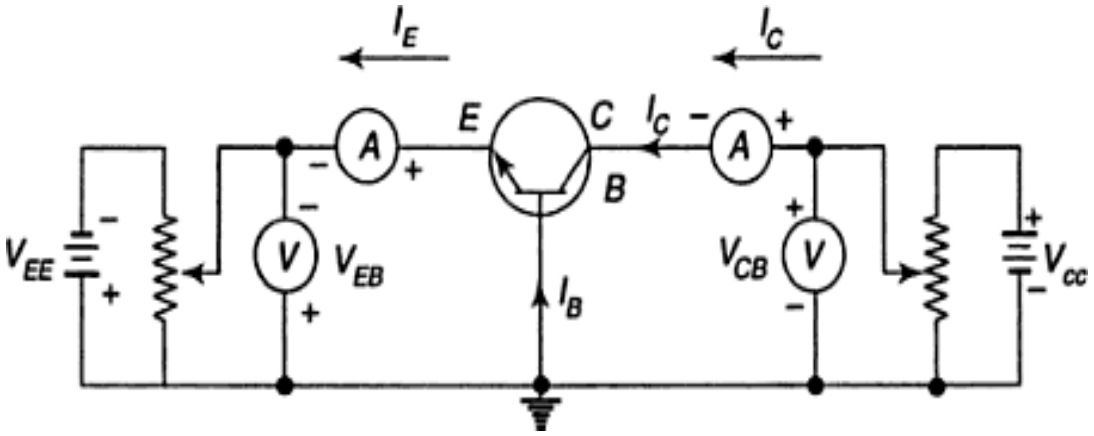
The collector current is therefore of the following form:

$$I_C = I_{C,s}[\exp(\frac{V_{BE}}{nV_t}) - 1] \tag{6}$$

Where the $I_{C,s}$ is the collector saturation current.

CB CONFIGURATION

In common base configuration circuit is shown in figure. Here base is grounded and it is used as the common terminal for both input and output. It is also called as grounded base configuration. Emitter is used as a input terminal where as collector is the output terminal.



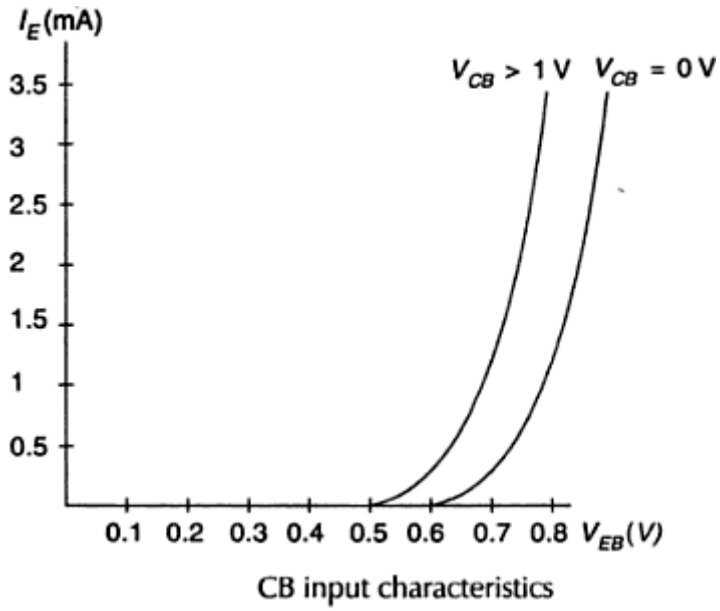
Input Characteristics

It is defined as the characteristic curve drawn between input voltage to input current whereas output voltage is constant.

To determine input characteristics, the collector base voltage V_{CB} is kept constant at zero and emitter current I_E is increased from zero by increasing V_{EB}.

This is repeated for higher fixed values of V_{CB}.

A curve is drawn between emitter current and emitter base voltage at constant collector base voltage is shown in figure.



CB input characteristics

When V_{CB} is zero EB junction is forward biased. So it behaves as a diode so that emitter current increases rapidly.

Output Characteristics

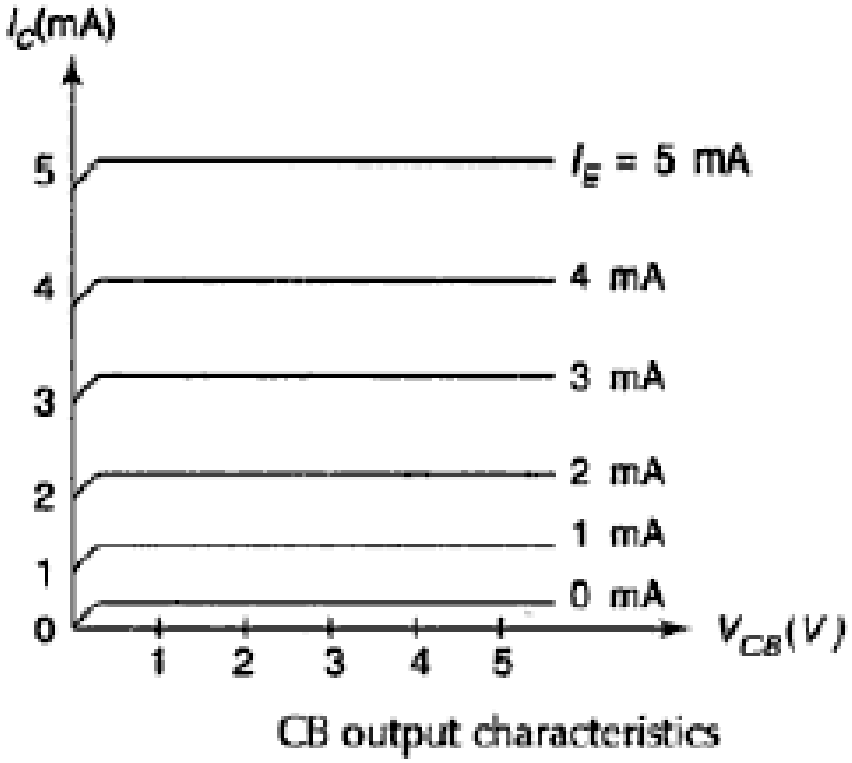
It is defined as the characteristic curve drawn between output voltage to output current whereas input current is constant.

To determine output characteristics, the emitter current I_E is kept constant at zero and collector current Ic is increased from zero by increasing V_{CB}.

This is repeated for higher fixed values of I_E.

From the characteristic it is seen that for a constant value of I_E, Ic is independent of V_{CB} and the curves are parallel to the axis of V_{CB}.

As the emitter base junction is forward biased the majority carriers that is electrons from the emitter region are injected into the base region.



CB output characteristics

In CB configuration a variation of the base-collector voltage results in a variation of the quasi-neutral width in the base. The gradient of the minority-carrier density in the base therefore changes, yielding an increased collector current as the collector-base current is increased. This effect is referred to as the Early effect.

Transistor parameters in CB configuration

The slope of CB characteristics will give the following four transistor parameters. It is known as base hybrid parameters.

I. Input impedance (h_{ib}): It is defined as the ratio of change in input voltage (emitter voltage) to change in input current (emitter current) with the output voltage (collector voltage) is kept constant.

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}, \; V_{CB} \text{ constant}$$

This ranges from 20ohms to 50ohms.

II. Output admittance (h_{ob}): It is defined as the ratio of change in output current (collector current) to change in output voltage (collector voltage) with the input current (emitter current) is kept constant.

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}, \; I_E \text{ constant}$$

This ranges from 0.1 to 10μ mhos.

III. Forward current gain (h_{fb}): It is defined as the ratio of change in output current (collector current) to change in input current (emitter current) with the output voltage (collector voltage) is kept constant.

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}, \; V_{CB} \text{ constant.}$$

This ranges from 0.9 to 1.0.

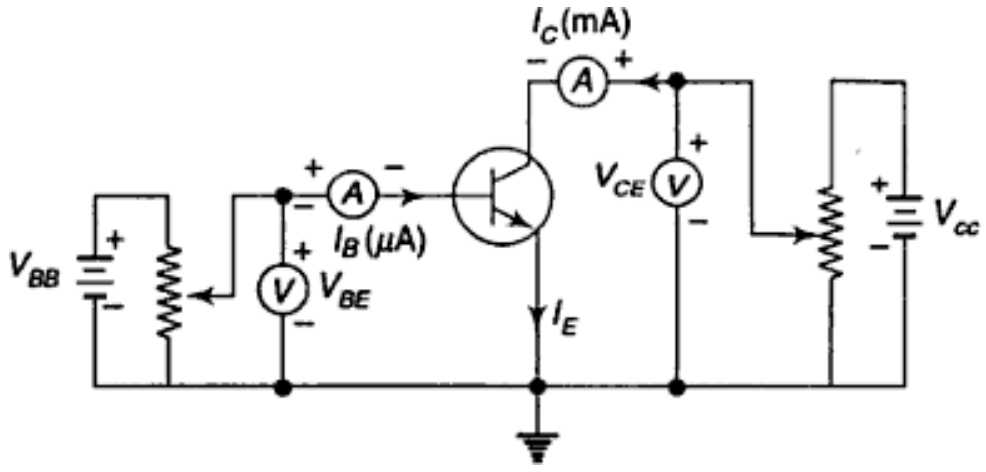
IV. Reverse voltage gain (h_{rb}): It is defined as the ratio of change in input voltage (emitter voltage) to change in output voltage (collector voltage) with the input current (emitter current) is kept constant.

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, \; I_E \text{ constant}$$

This ranges from 10^{-5} to 10^{-4}.

CE CONFIGURATION

In common emitter configuration circuit is shown in figure. Here emitter is grounded and it is used as the common terminal for both input and output. It is also called as grounded emitter configuration. Base is used as a input terminal whereas collector is the output terminal.



Input Characteristics

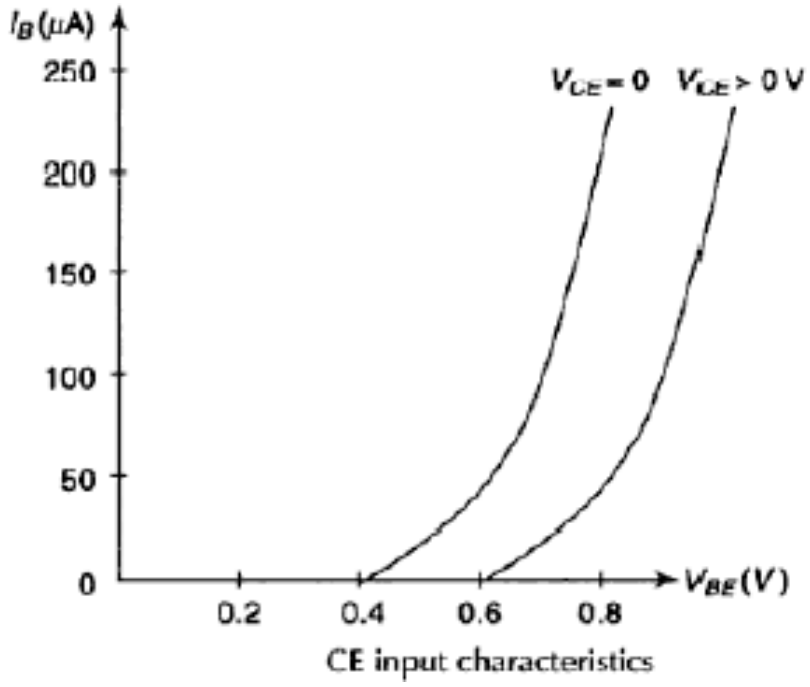
It is defined as the characteristic curve drawn between input voltage to input current whereas output voltage is constant.

To determine input characteristics, the collector base voltage V_{CB} is kept constant at zero and base current I_B is increased from zero by increasing V_{BE}.

This is repeated for higher fixed values of V_{CE}.

A curve is drawn between base current and base emitter voltage at constant collector base voltage is shown in figure.

.



CE input characteristics

Here the base width decreases. So curve moves right as V_{CE} increases.

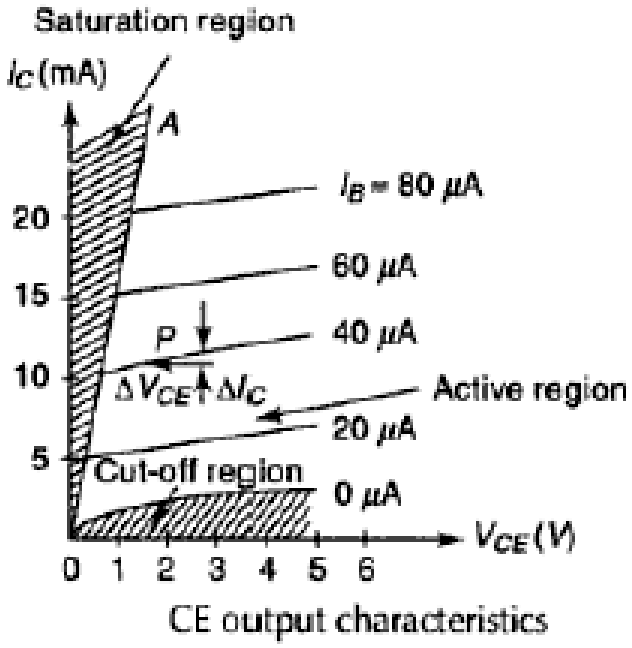
Output Characteristics

It is defined as the characteristic curve drawn between output voltage to output current whereas input current is constant.

To determine output characteristics, the base current I_B is kept constant at zero and collector current Ic is increased from zero by increasing V_{CE}.

This is repeated for higher fixed values of $I_{B..}$

From the characteristic it is seen that for a constant value of I_B, Ic is independent of V_{CB} and the curves are parallel to the axis of V_{CE}.



CE output characteristics

The output characteristic has 3 basic regions:

- Active region –defined by the biasing arrangements

- Cutoff region – region where the collector current is 0A

- Saturation region- region of the characteristics to the left of VCB = 0V

Active region	Saturation region	Cut-off region
•I_E increased, Ic increased •BE junction forward bias and CB junction reverse bias •Refer to the graf, Ic ≈ I_E •Ic not depends on V_{CB} •Suitable region for the transistor working as amplifier	• BE and CB junction is forward bias • Small changes in V_{CB} will cause big different to Ic • The allocation for this region is to the left of V_{CB}= 0 V.	• Region below the line of I_E=0 A • BE and CB is reverse bias • no current flow at collector, only leakage current

Transistor parameters in CE configuration

The slope of CE characteristics will give the following four transistor parameters. It is known as emitter hybrid parameters.

I. Input impedance (h_{ie}): It is defined as the ratio of change in input voltage (base voltage) to change in input current (base current) with the output voltage (collector voltage) is kept constant.

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}, \; V_{CE} \text{ constant}$$

This ranges from 500ohms to 2000ohms.

II. Output admittance (h_{oe}): It is defined as the ratio of change in output current (collector current) to change in output voltage (collector voltage) with the input current (base current) is kept constant.

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}, \; I_B \text{ constant}$$

This ranges from 0.1 to 10μ mhos.

III. Forward current gain (h_{fe}): It is defined as the ratio of change in output current (collector current) to change in input current (base current) with the output voltage (collector voltage) is kept constant.

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}, \; V_{CE} \text{ constant}$$

This ranges from 20 to 200.

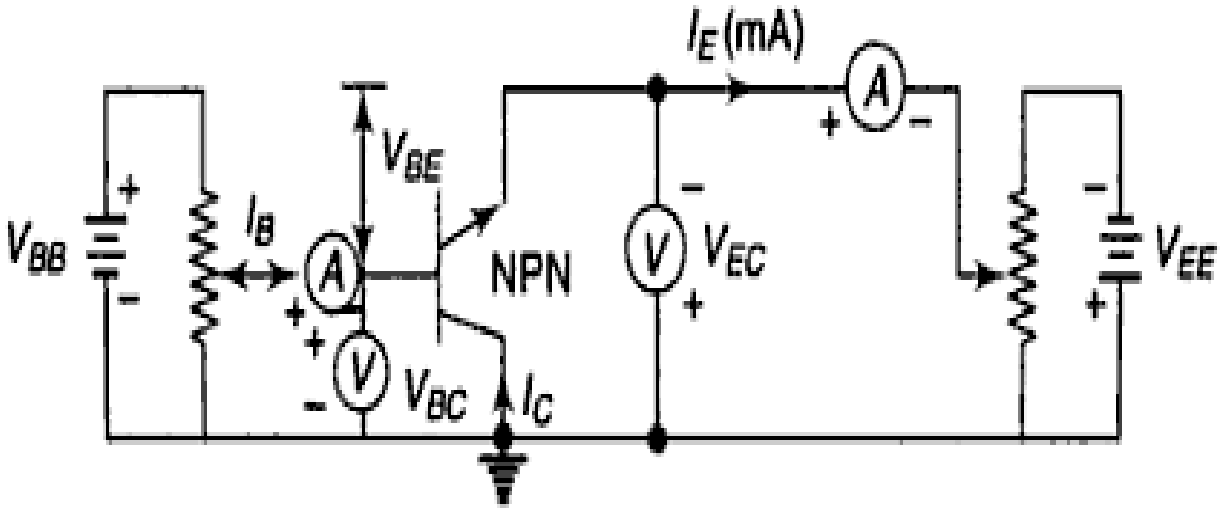
IV. Reverse voltage gain (h_{re}): It is defined as the ratio of change in input voltage (base voltage) to change in output voltage (collector voltage) with the input current (base current) is kept constant.

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}, \; I_B \text{ constant}$$

This ranges from 10^{-5} to 10^{-4}.

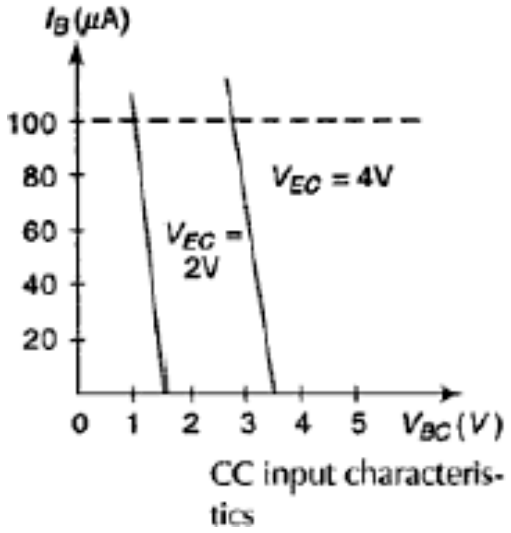
CC CONFIGURATION

In common collector configuration circuit is shown in figure. Here collector is grounded and it is used as the common terminal for both input and output. It is also called as grounded collector configuration. Base is used as a input terminal whereas emitter is the output terminal.



Input Characteristics

It is defined as the characteristic curve drawn between input voltage to input current whereas output voltage is constant.



CC input characteristics

To determine input characteristics, the emitter base voltage V_{EB} is kept constant at zero and base current I_B is increased from zero by increasing V_{BC}.

This is repeated for higher fixed values of V_{CE}.

A curve is drawn between base current and base emitter voltage at constant collector base voltage is shown in above figure.

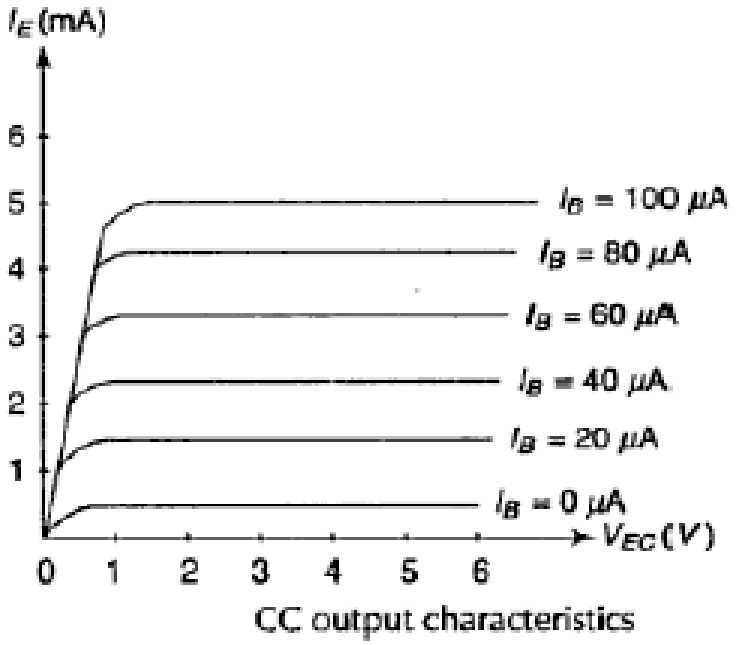
Output Characteristics

It is defined as the characteristic curve drawn between output voltage to output current whereas input current is constant.

To determine output characteristics, the base current I_B is kept constant at zero and emitter current I_E is increased from zero by increasing V_{EC}.

This is repeated for higher fixed values of I_B.

From the characteristic it is seen that for a constant value of I_B, I_E is independent of V_{EB} and the curves are parallel to the axis of V_{EC}.



CC output characteristics

Transistor parameters in CC configuration

The slope of CC characteristics will give the following four transistor parameters. It is known as base hybrid parameters.

I. Input impedance (h_{ic}): It is defined as the ratio of change in input voltage (base voltage) to change in input current (base current) with the output voltage (emitter voltage) is kept constant.

$$h_{ic} = \frac{\Delta V_{BC}}{\Delta I_B}, \; V_{EC} \text{ constant}$$

II. Output admittance (h_{oc}): It is defined as the ratio of change in output current (emitter current) to change in output voltage (emitter voltage) with the input current (base current) is kept constant.

$$h_{oc} = \frac{\Delta I_E}{\Delta V_{EC}}, \; I_B \text{ constant}$$

III. Forward current gain (h_{fc}): It is defined as the ratio of change in output current (emitter current) to change in input current (base current) with the output voltage (emitter voltage) is kept constant.

$$h_{fc} = \frac{\Delta I_E}{\Delta I_B}, \; V_{EC} \text{ constant}$$

IV. Reverse voltage gain (h_{rc}): It is defined as the ratio of change in input voltage (base voltage) to change in output voltage (emitter voltage) with the input current (base current) is kept constant.

$$h_{rc} = \frac{\Delta V_{BC}}{\Delta V_{EC}}, \; I_B \text{ constant}$$

A comparison of CB, CE and CC Configurations

Property	*CB*	*CE*	*CC*
Input resistance	Low (about 100 Ω)	Moderate (about 750 Ω)	High (about 750 kΩ)
Output resistance	High (about 450 kΩ)	Moderate (about 45 kΩ)	Low (about 25 Ω)
Current gain	1	High	High
Voltage gain	About 150	About 500	Less than 1
Phase shift between input & output voltages	0 or 360°	180°	0 or 360°
Applications	for high frequency circuits	for audio frequency circuits	for impedance matching

Hybrid-Pi Model

Bipolar transistors are commonly used in circuits that amplify time-varying or sinusoidal signals. In these linear amplifier circuits, the transistor is biased in the forward-active region and small sinusoidal voltages and currents are superimposed on dc voltages and currents. In these applications, the sinusoidal parameters are of interest, so it is convenient to develop a small-signal equivalent circuit of the bipolar transistor using the small-signal admittance parameters of the pn junction.

Figure 1a shows an npn bipolar transistor in a common emitter configuration with the small-signal terminal voltages and currents. Figure 1b shows the cross section of the npn transistor. The C, B, and E terminals are the external connections to the transistor, while the C', B', and E' points are the idealized internal collector, base, and emitter regions.

We can begin constructing the equivalent circuit of the transistor by considering the various terminals individually. Figure 2a shows the equivalent circuit between the external input base terminal and the external emitter terminal. The résistance rb is the series resistance in the base between the external base terminal B and the internal base region B'. The B'-E' junction is forward biased, so C, is the junction diffusion capacitance and r, is the junction diffusion resistance. The diffusion capacitance C is,

$$C_d = \left(\frac{1}{2V_t}\right)(I_{p0}\tau_{p0} + I_{n0}\tau_{n0})$$

the diffusion resistance r,

$$r = \frac{V}{I_{DQ}}$$

The values of both parameters are functions of the junction current. These two elements are in parallel with the junction capacitance, which is C. Finally, r is the series resistance between the external emitter terminal and the internal emitter region. This resistance is usually very small and may be on the order of 1 to2 Ω.

Figure 2b shows the equivalent circuit looking into the collector terminal. The ***r,*** resistance is the series resistance between the external and internal collector connections and the capacitance **C,** is the junction capacitance of the reverse-biased collector-substrate junction

Figure 3 shows the equivalent circuit of the reverse-biased B'-C' junction. The C, parameter is the reverse-biased junction capacitance and r, is the 1 reverse-biased diffusion resistance.

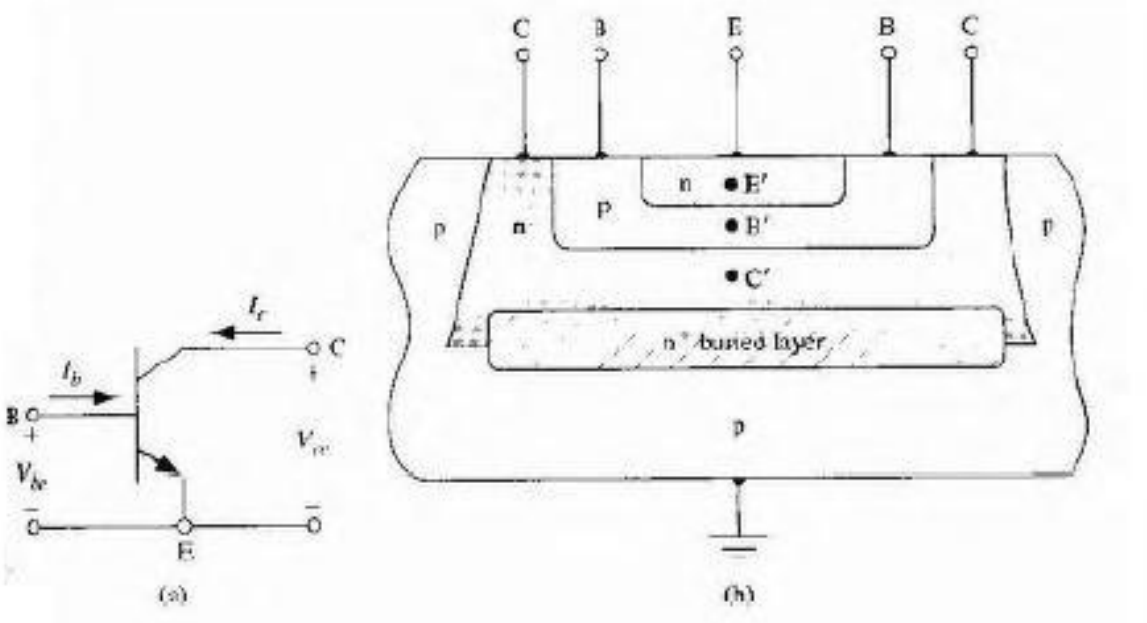
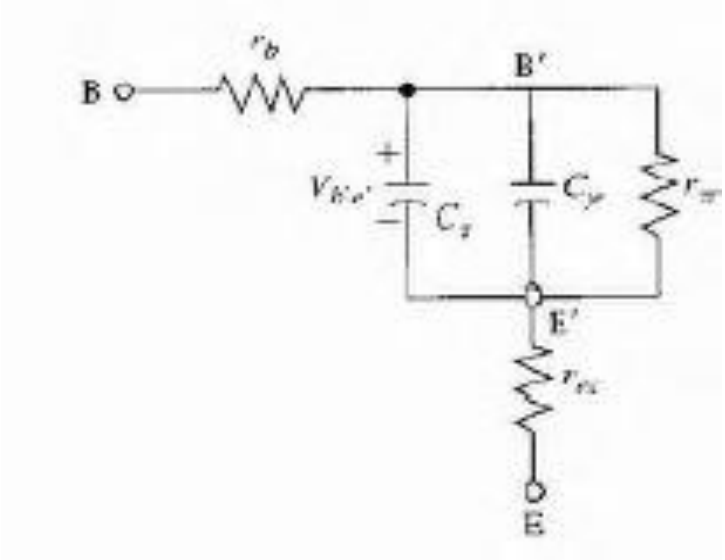


Figure 1 | (a) Common emitter npn bipolar transistor with small-signal current and voltages. (b) Cross section of an npn bipolar transistor for the hybrid-pi model.



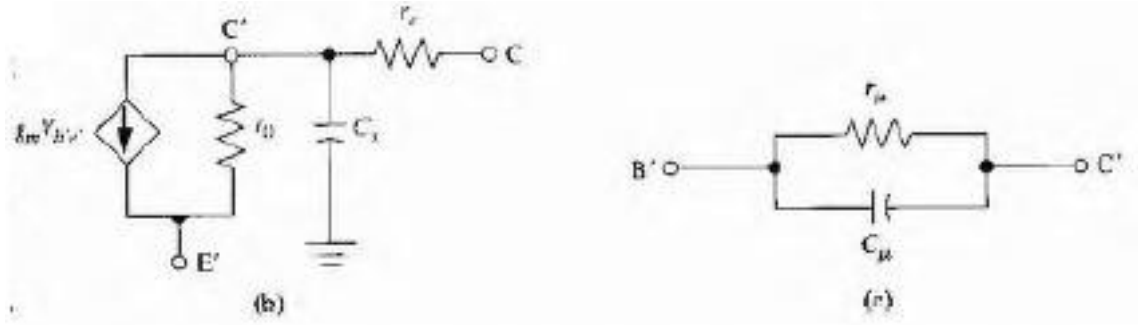


Figure 2 | Components of the hybrid-pi equivalent circuit between (a) the base and emitter, (b) the collector and emitter, and (c) the base and collector.

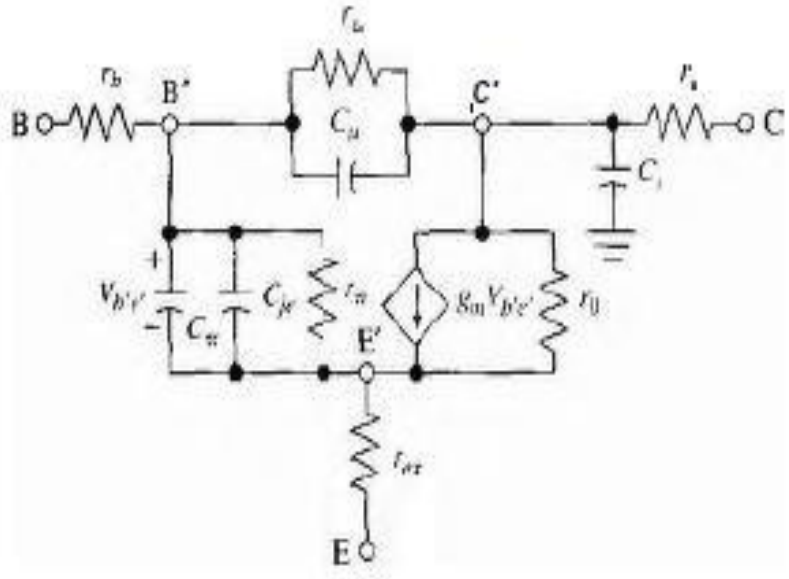


Figure 3 Hybrid-pi equivalent circuit.

Figure 3 shows the complete hybrid-pi equivalent circuit. A computer simulation is usually required for this complete model because of the large number of elements. However, some simplifications can be made in order to gain an appreciation for the frequency effects of the bipolar transistor.

h-PARAMETER BJT MODEL

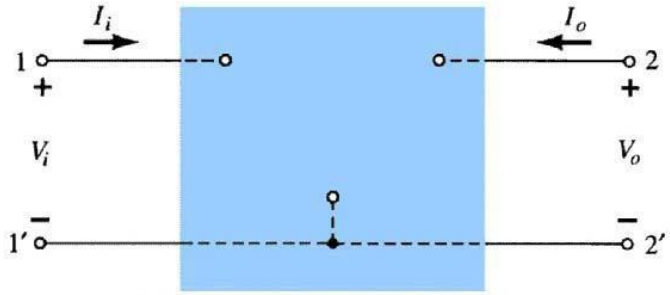
The h-parameter model is typically suited to transistor circuit modeling. It is important because:

1. its values are used on specification sheets
2. it is one model that may be used to analyze circuit behavior
3. it may be used to form the basis of a more accurate transistor model

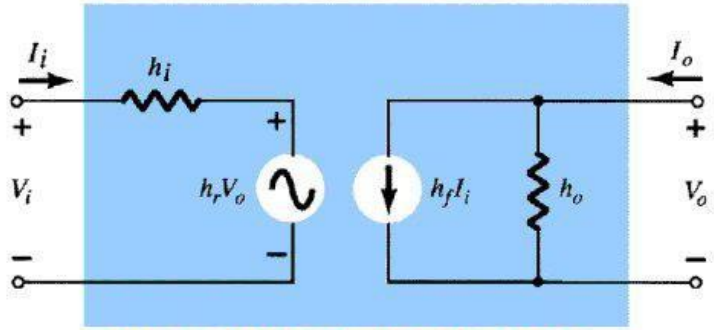
The h parameter model has values that are complex numbers that vary as a function of:

1. Frequency
2. Ambient temperature
3. Q-Point

The revised two port network for the h parameter model is shown on the right. At low and mid-band frequencies, the h parameter values are real values. Other models exist because this model is not suited for circuit analysis at high frequencies



Hybrid Equivalent Model



Hybrid Equivalent Circuit

The h-parameter model is defined by:

$$\begin{vmatrix} V_1 \\ I_2 \end{vmatrix} = \begin{vmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{vmatrix} \begin{vmatrix} I_1 \\ V_2 \end{vmatrix}$$

$$V1 = h11I1 + h12V2 \quad (KVL)$$
$$I2 = h21I1 + h22V2 \quad (KCL)$$

The h-parameter model for the common emitter circuit is on the fig. On spec sheet:

h11 = hix
h12 = hrx
h21 = hfx
h22 = hox

hrx and hfx are dimensionless ratios

hix is an impedance <Ω>

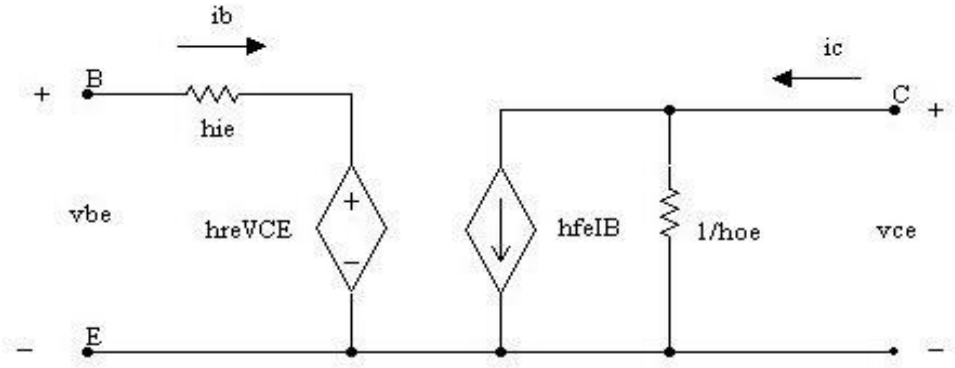
hox is an admittance <S>

where x = lead based on circuit configuration

e = emitter for common emitter

c = collector for common collector

b = base for common base

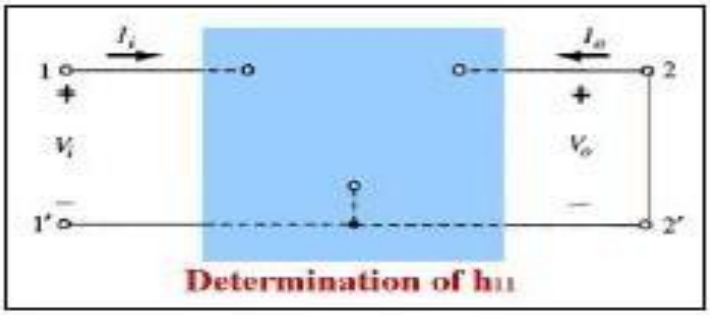


Short Circuit Input Impedance

h_{11} = Z_{IN} with output shorted <Ω>

$$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_O = 0}$$

1. Short terminals 2 2'
2. Apply test source V_i to terminal 1 1'
3. Measure I_i
4. Calculate h_{11}

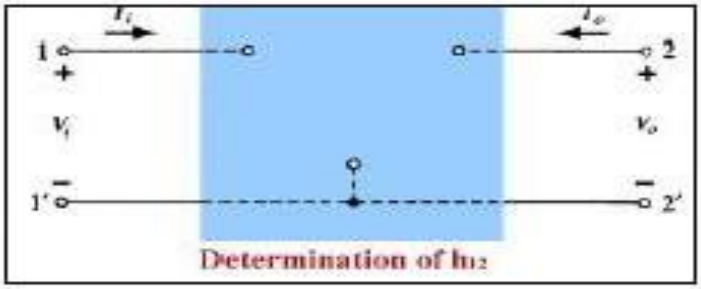


Open Circuit Reverse Transfer Ratio

h_{12} <dimensionless>

$$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i = 0}$$

1. Open terminals 1 1'
2. Apply test source V_2 to terminal 2 2'
3. Measure V_i
4. Measure V_o
5. Calculate h_{12}

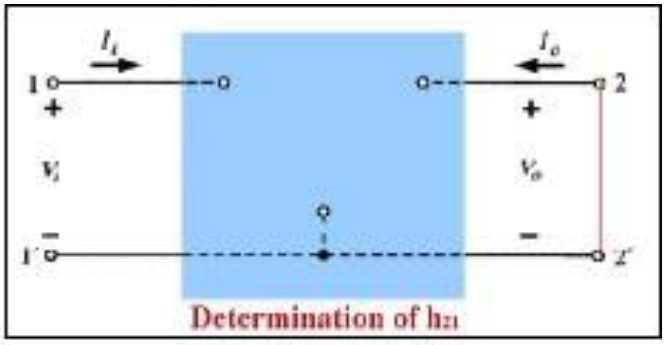


Short Circuit Forward Transfer Ratio

h_{21} = <dimensionless>

$$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_O = 0}$$

1. Short terminals 2 2'
2. Apply test source V_i to terminal 1 1'
3. Measure I_i
4. Measure I_o
5. Calculate h_{21}

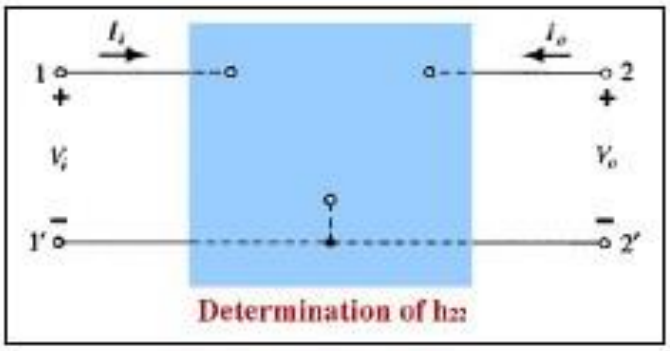


Open Circuit Output Admittance

h_{22} <Siemans>

$$h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i = 0}$$

1. Open terminals 1 1'
2. Apply test source V_2 to terminal 2 2'
3. Measure I_o
4. Measure V_o
5. Calculate h_2



Determination of h_{22}

Ebers-Moll Model

The Ebers-Moll model, or equivalent circuit, is one of the classic models of the bipolar transistor. This particular model is based on the interacting diode junctions and applicable in any of the transistor operating modes. Figure shows the current directions and voltage polarities used in the Ebers Moll model. The currents are defined as all entering the terminals so that

$I_E + I_B + Ic = 0$

The direction of the emitter current is opposite to what we have considered up to point, but as long as we are consistent in the analysis, the defined direction does not matter.

The collector current can be written in general as

$Ic = \alpha_F I_F - I_R$

where α_F is the common base current rain in the forward-active mode. In this **mode.**

$$I_C = \alpha_F I_F + I_{CS}$$

where the current *lcs* is the reverse-bias B-C junction current. The current is given by

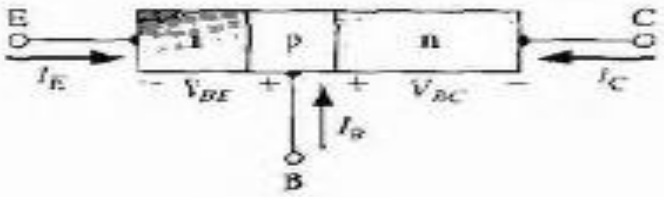
$$I_F = I_{ES}\left[\exp\left(\frac{eV_{BE}}{kT}\right) - 1\right]$$

If the B-C junction becomes forward biased, such as in saturation, then we can write the current *IR* as

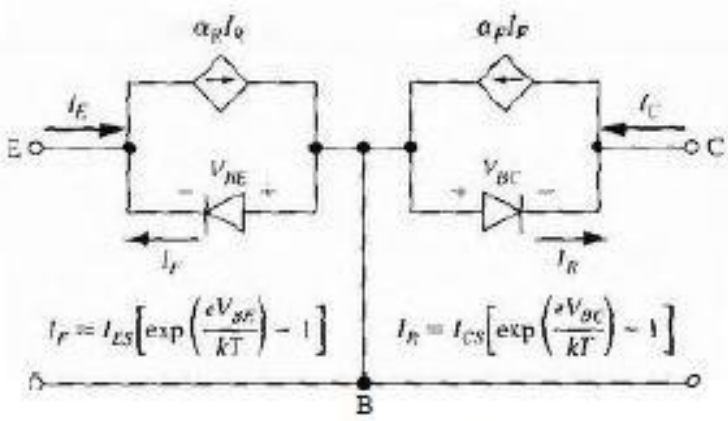
$$I_R = I_{CS}\left[\exp\left(\frac{eV_{BC}}{kT}\right) - 1\right]$$

Using above equations collector current written as

$$I_C = \alpha_F I_{ES}\left[\exp\left(\frac{eV_{BE}}{kT}\right) - 1\right] - I_{CS}\left[\exp\left(\frac{eV_{BC}}{kT}\right) - 1\right]$$



Current direction and voltage polarity definitions lor the Ebers–Moll model.



Basic Ebers–Moll equivalent circuit.

We can also write the emitter current as

$$I_E = \alpha_R I_R - I_F$$

$$I_E = \alpha_R I_{CS}\left[\exp\left(\frac{eV_{BC}}{kT}\right) - 1\right] - I_{ES}\left[\exp\left(\frac{eV_{BE}}{kT}\right) - 1\right]$$

The current sources in the equivalent circuit represent current components that depend on voltages across other junctions. The Ebers-Moll model has four parameters: α_F, α_R, I_{ES} and lcs.
However, only three parameters are independent. The reciprocity relationship states that

$$\alpha_F I_{ES} = \alpha_R I_{CS}$$

Normally in electronic circuit applications, the collector-emitter voltage at saturation is of interest. We can define the C-E saturation voltage as

$$V_{CE}(\text{sat}) = V_{BE} - V_{BC}$$

Combining the previous some eqn we get

$$-(I_B + I_C) = \alpha_R I_{CS}\left[\exp\left(\mathbf{f}\right) - 1\right] - I_{ES}\left[\exp\left(\frac{eV_{BE}}{kT}\right) - 1\right]$$

If we solve for the value of $[\exp(eV_{BC}/kT) - 1]$ and sub in previous one and simplifying we get

$$V_{BE} = V_t \ln\left[\frac{I_C(1-\alpha_R) + I_B + I_{ES}(1-\alpha_F\alpha_R)}{I_{ES}(1-\alpha_F\alpha_R)}\right]$$

where Vs, is the thermal voltage. IIIly we solve $[\exp(eV_{BE}/kT) - 1]$ and substitute it, we get

$$V_{BC} = V_t \ln\left[\frac{\alpha_F I_B - (1-\alpha_F)I_C + I_{CS}(1-\alpha_F\alpha_R)}{I_{CS}(1-\alpha_F\alpha_R)}\right]$$

We may neglect the I_{ES} and I_{CS} and we get

$$V_{CE}(\text{sat}) = V_{BE} - V_{CB} = V_t \ln\left[\frac{I_C(1-\alpha_R) + I_B}{\alpha_F I_B - (1-\alpha_F)I_C} \cdot \frac{I_{CS}}{I_{ES}}\right]$$

The ratio of Ics to I_{ES} can be written in terms of α_F and α_R and we finally get

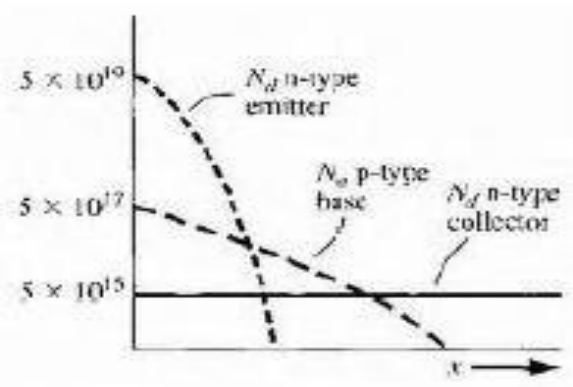
$$V_{CE}(\text{sat}) = V_t \ln\left[\frac{I_C(1-\alpha_R) + I_B}{\alpha_F I_B - (1-\alpha_F)I_C} \cdot \frac{\alpha_F}{\alpha_R}\right]$$

Gummel-Poon Model

The Gummel-Poon model of the BIT considers more physics of the transistor that the Ebers-Moll model. This model can he used if, for example, there is a non-uniform doping concentration in the base.

The electron current density in the base of m npn transistor can be written as

$$J_n = e\mu_n n(x)\mathrm{E} + eD_n \frac{dn(x)}{dx}$$



Impurity concentration profiles of a double-diffused npn bipolar transistor.

An electric field will occur in the base if non uniform doping exists in the base. Electric field can be written as

$$\mathrm{E} = \frac{kT}{e} \cdot \frac{1}{p(x)} \cdot \frac{dp(x)}{dx}$$

where p(x) is the majority carrier hole concentration in the base.
Under low injection, the hole concentration is just the acceptor impurity concentration.
With the doping profile shown in Figure.The electric field is negative (from the collector to the emitter). The direction of this electric field aids the flow of electrons across the base.

Substituting previous Equation we get

$$J_n = e\mu_n n(x) \cdot \frac{kT}{e} \cdot \frac{1}{p(x)} \cdot \frac{dp(x)}{dx} + eD_n \frac{dn(x)}{dx}$$

Using Einstein's relation, we can write Equation in the form

$$J_n = \frac{eD_n}{p(x)}\left(n(x)\frac{dp(x)}{dx} + p(x)\frac{dn(x)}{dx}\right) - \frac{eD_n}{p(x)}\cdot\frac{d(pn)}{dx}$$

It is written in the form of

$$\frac{J_n p(x)}{eD_n} = \frac{d(pn)}{dx}$$

Integrating this eqn through the base

$$\frac{J_n}{eD_n}\int_0^{x_B} p(x)\,dx = \int_0^{x_B}\frac{dp(x)}{dx}\,dx = p(x_B)n(x_B) - p(0)n(0)$$

The integral in the denominator is the total majority carrier charge in the base and is known as the base Gummel number; defined as Q_B.

The hole current density in the emitter of an npn transistor can be expressed as,

$$J_p = \frac{-eD_p n_i^2 \exp(V_{BE}/V_t)}{\int_0^{x_E} n(x')\,dx'}$$

With the doping profile shown in Figure. The electric field is negative (from the collector to the emitter). The direction of this electric field aids the flow of electrons across the base.

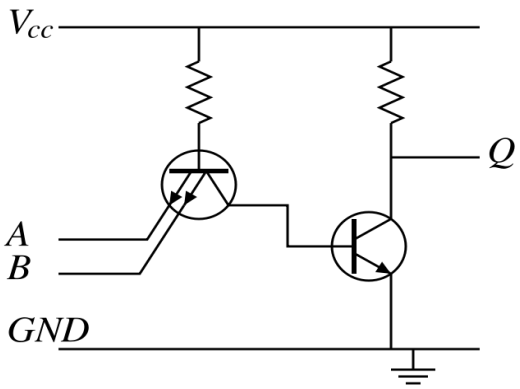
The integral in the denominator is the total majority carrier charge in the emitter and is known as the emitter Gummel number, defined as Q_E.

The Gummel-Poon model can also take into account non ideal effects, such as the Early effect and high-level injection.

If the B-E voltage becomes too large. low injection no longer applies, which leads to high-level injection. In this case, the total hole concentration in the base increases because of the increased excess hole concentration. This means that the base Gummel number will increase.

The Gummel-Poon model can then he used to describe the basic operation of the transistor as well as to describe non ideal effects.

Multi Emitter Transistor (Transistor Transistor Logic)



TTL inputs are the emitters of a multiple-emitter transistor. This IC structure is functionally equivalent to multiple transistors where the bases and collectors are tied together. The output is buffered by a common emitter amplifier.

Inputs both logical ones. When all the inputs are held at high voltage, the base–emitter junctions of the multiple-emitter transistor are reverse-biased. Unlike DTL, a small ‒collector‖ current (approximately 10μA) is drawn by each of the inputs. This is because the transistor is in reverse-active mode. An approximately constant current flows from the positive rail, through the resistor and into the base of the multiple emitter transistor. This current passes through the base-emitter junction of the output transistor, allowing it to conduct and pulling the output voltage low (logical zero).

An input logical zero. Note that the base-collector junction of the multiple-emitter transistor and the base-emitter junction of the output transistor are in series between the bottom of the resistor and ground. If one input voltage becomes zero, the corresponding base-emitter junction of the multiple-emitter transistor is in parallel with these two junctions. A phenomenon called current steering means that when two voltage-stable elements with different threshold voltages are connected in parallel, the current flows through the path with the smaller threshold voltage. As a result, no current flows through the base of the output transistor, causing it to stop conducting and the output voltage becomes high (logical one). During the transition the input transistor is briefly in its active region; so it draws a large current away from the base of the output transistor and thus quickly discharges its base. This is a critical advantage of TTL over DTL that speeds up the transition over a diode input structure.

The main disadvantage of TTL with a simple output stage is the relatively high output resistance at output logical "1" that is completely determined by the output collector resistor. It limits the number of inputs that can be connected (the fanout). Some advantage of the simple output stage is the high voltage level (up to V_{CC}) of the output logical "1" when the output is not loaded.

UNIT III

FIELD EFFECT TRANSISTORS

Field effect devices are those in which current is controlled by the action of an electron field, rather than carrier injection.

Field-effect transistors are so named because a weak electrical signal coming in through one electrode creates an electrical field through the rest of the transistor.

The FET was known as a ‐unipolar‖ transistor because the function depends only on minority carriers.

The term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

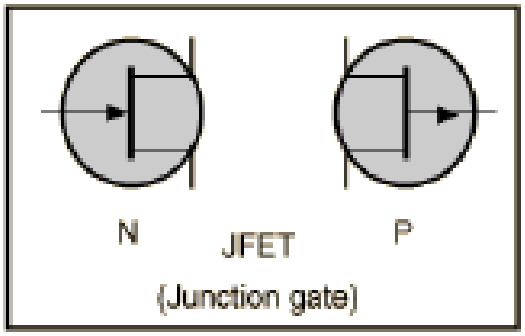
The family of FET devices may be divided into :

• Junction FET

• Depletion Mode MOSFET

Enhancement Mode MOSFET

Junction FETs (JFETs)



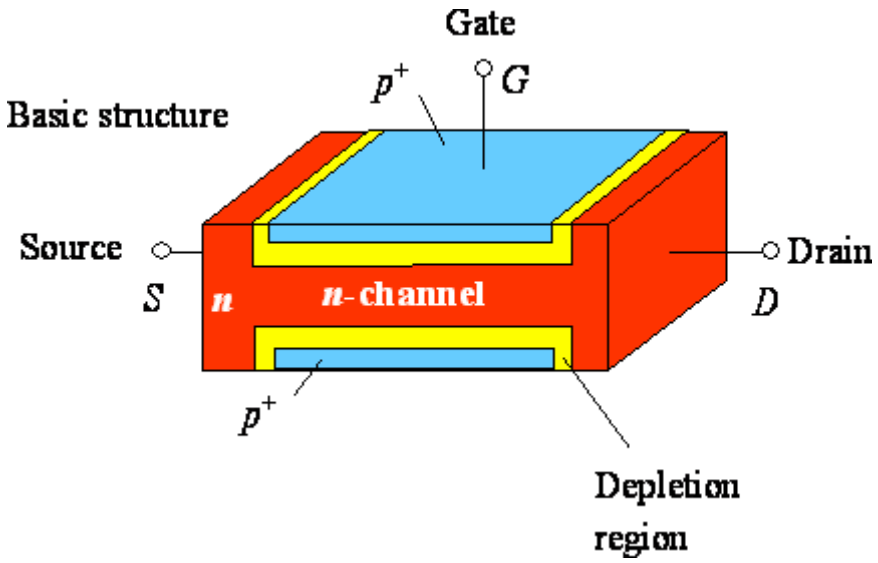
JFETs consists of a piece of high-resistivity semiconductor material (usually Si) which constitutes a channel for the majority carrier flow.

Conducting semiconductor channel between two ohmic contacts – source & drain.

JFET is a high-input resistance device, while the BJT is comparatively low.

If the channel is doped with a donor impurity, n-type material is formed and the channel current will consist of electrons.

If the channel is doped with an acceptor impurity, p-type material will be formed and the channel current will consist of holes.



N-channel devices have greater conductivity than p-channel types, since electrons have higher mobility than do holes; thus n-channel JFETs are approximately twice as efficient conductors compared to their p-channel counterparts.

The magnitude of this current is controlled by a voltage applied to a gate, which is a reverse-biased.

The fundamental difference between JFET and BJT devices: when the JFET junction is reverse-biased the gate current is practically zero, whereas the base current of the BJT is always some value greater than zero.

Basic structure of JFETs

• In addition to the channel, a JFET contains two ohmic contacts: the source and the drain.

• The JFET will conduct current equally well in either direction and the source and drain leads are usually interchangeable. N-channel JFET

• This transistor is made by forming a channel of N-type material in a P-type substrate.

• Three wires are then connected to the device.

• One at each end of the channel.

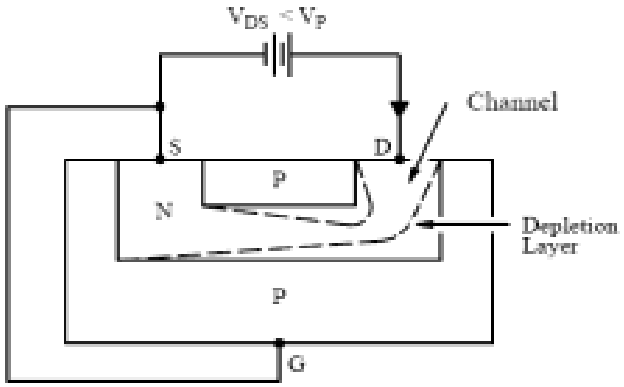
• One connected to the substrate.

In a sense, the device is a bit like a PN-junction diode, except that there are two wires connected to the N-type side

• The gate is connected to the source.

• Since the pn junction is reverse-biased, little current will flow in the gate connection.

• The potential gradient established will form a depletion layer, where almost all the electrons present in the n-type channel will be swept away. The most depleted portion is in the high field between the G and the D, and the least-depleted area is between the G and the S.



• Because the flow of current along the channel from the (+ve) drain to the (-ve) source is really a flow of free electrons from S to D in the n-type Si, the magnitude of this current will fall as more Si becomes depleted of free electrons.

• There is a limit to the drain current (ID) which increased VDS can drive through the channel.

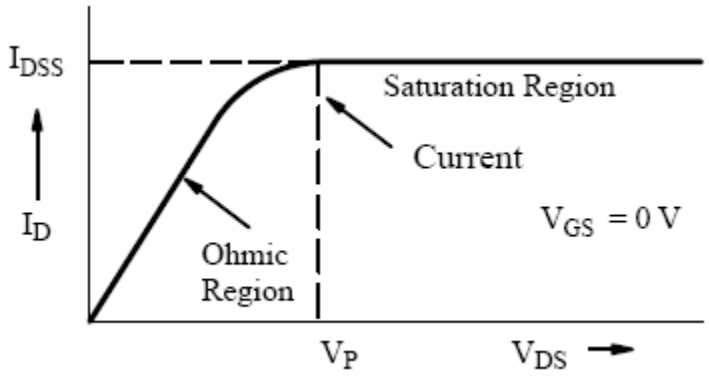
• This limiting current is known as IDSS (*Drain-to-Source current with the gate shorted to the source*).

• The output characteristics of an n-channel JFET with the gate short-circuited to the source.

• The initial rise in ID is related to the buildup of the depletion layer as VDS increases.

• The curve approaches the level of the limiting current IDSS when ID begins to be pinched off.

• The physical meaning of this term leads to one definition of pinch-off voltage, VP , which is the value of VDS at which the maximum IDSS flows.



• With a steady gate-source voltage of 1 V there is always 1 V across the wall of the channel at the source end.

• A drain-source voltage of 1 V means that there will be 2 V across the wall at the drain end. (The drain is ‗up' 1V from the source potential and the gate is 1V ‗down', hence the total difference is 2V.)

• The higher voltage difference at the drain end means that the electron channel is squeezed down a bit more at this end.

• When the drain-source voltage is increased to 10V the voltage across the channel walls at the drain end increases to 11V, but remains just 1V at the source end.

• The field across the walls near the drain end is now a lot larger than at the source end.

• As a result the channel near the drain is squeezed down quite a lot.

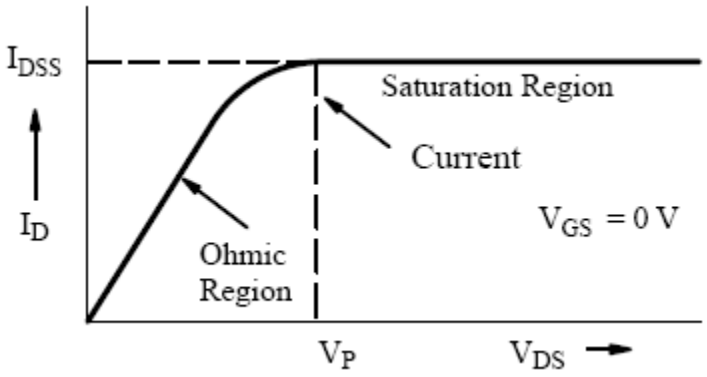
• Increasing the source-drain voltage to 20V squeezes down this end of the channel still more.

• As we increase this voltage we increase the electric field which drives electrons along the open part of the channel.

• However, also squeezes down the channel near the drain end.

• This reduction in the open channel width makes it harder for electrons to pass.

• As a result the drain-source current tends to remain constant when we increase the drain source voltage.



• Increasing VDS increases the widths of depletion layers, which penetrate more into channel and hence result in more channel narrowing toward the drain.

• The resistance of the n-channel, RAB therefore increases with VDS.

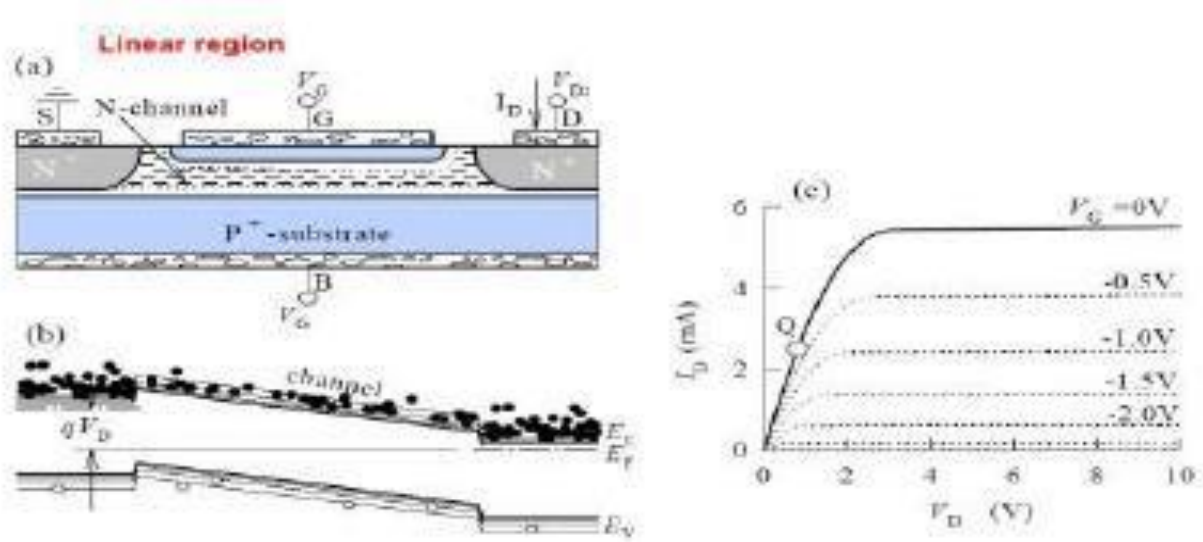
• The drain current: IDS = VDS/RAB

• ID versus VDS exhibits a sub linear behavior, see figure for VDS < 5V.

• The pinch-off voltage, VP is the magnitude of reverse bias needed across the p+n junction to make them just touch at the drain end.

• Since actual bias voltage across p+n junction at drain end is VGD, the pinch-off occur whenever: VGD = -VP.

JFET: I-V characteristics



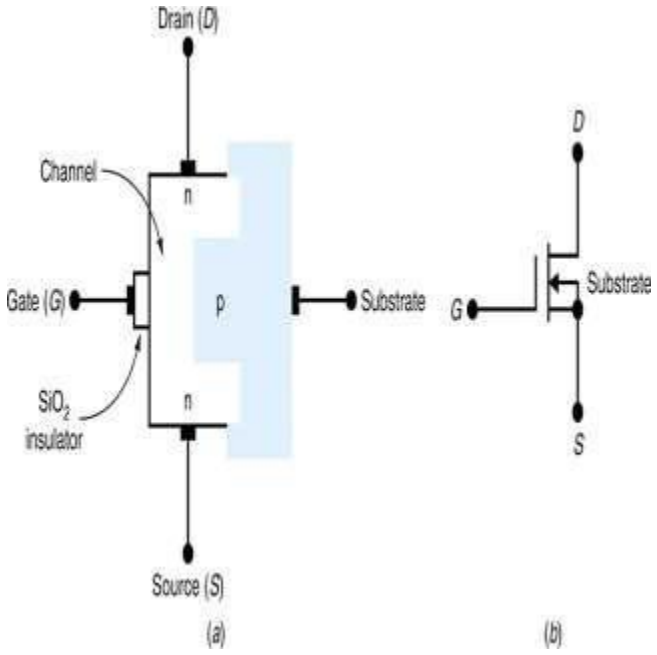
<u>MOSFETs and Their Characteristics</u>

The metal-oxide semiconductor field effect transistor has a gate, source, and drain just like the JFET.

The drain current in a MOSFET is controlled by the gate-source voltage VGS.
There are two basic types of MOSFETS: the enhancement-type and the depletion-type.

The enhancement-type MOSFET is usually referred to as an E-MOSFET, and the depletion type, a D-MOSFET.

The MOSFET is also referred to as an IGFET because the gate is insulated from the channel



DEPLETION-TYPE MOSFET

MOSFETs are further broken down into depletion type and enhancement type. The terms depletion and enhancement define their basic mode of operation, while the label MOSFET stands for metal-oxide-semiconductor-field-effect transistor.

Basic Construction

The basic construction of the n-channel depletion-type MOSFET is provided in Fig. A slab of p-type material is formed from a silicon base and is referred to as the substrate. It is the foundation upon which the device will be constructed. In some cases the substrate is internally

connected to the source terminal. However, many discrete devices provide an additional terminal labeled SS, resulting in a four-terminal device, such as that appearing in Fig. 1

The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO_2) layer.

SiO_2 is a particular type of insulator referred to as a dielectric that sets up opposing (as revealed by the prefix di-) electric fields within the dielectric when exposed to an externally applied field.

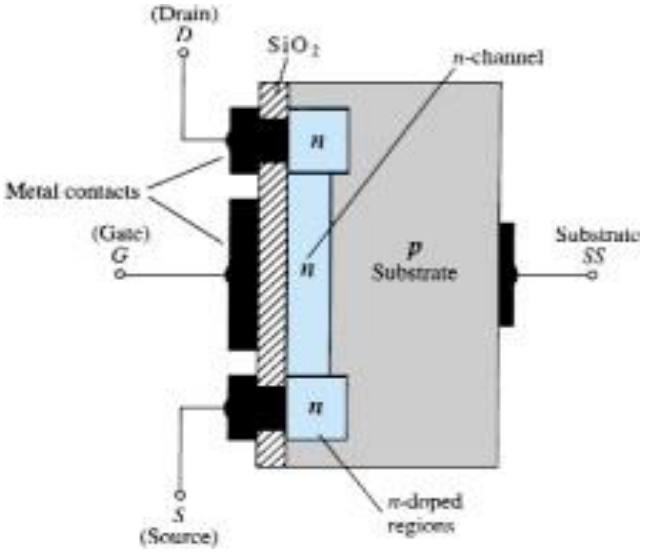


Fig. 1 n – channel depletion type MOSFET

There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

It is the insulating layer of SiO2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

Basic Operation and Characteristics

In Fig. 2 the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other, and a voltage VDS is applied across the drain-to-source terminals.

The result is an attraction for the positive potential at the drain by the free electrons of the n-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with V_{GS} = 0 V continues to be labeled IDSS, as shown in Fig. 3.

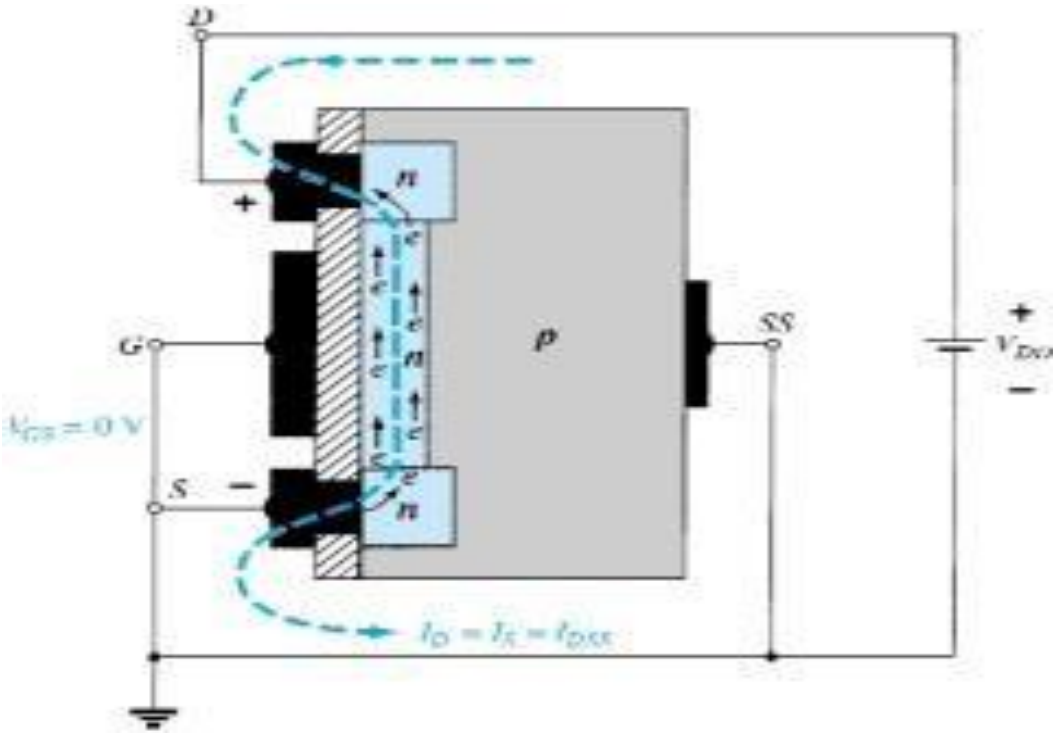


Fig 2. n – channel depletion type MOSFET with $V_{GS} = 0$ V

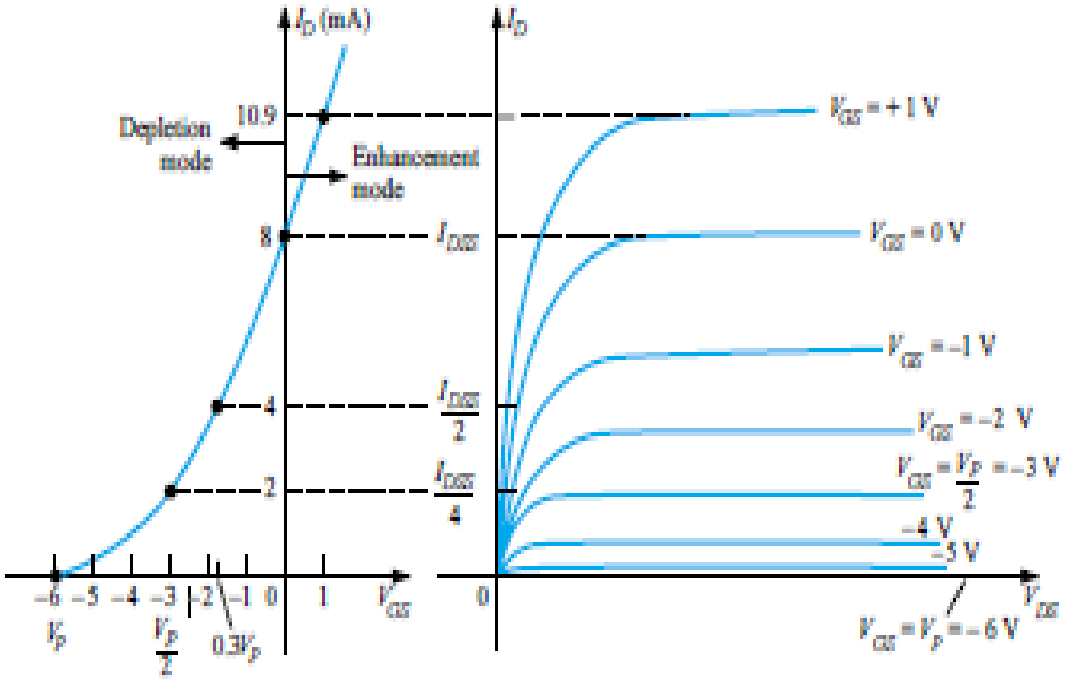


Fig 3. Drain and transfer characteristics

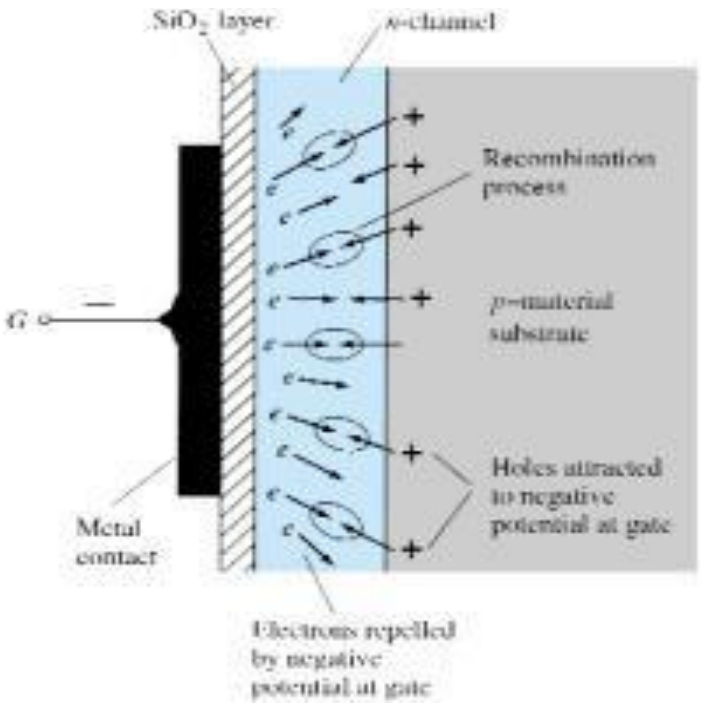


Fig.4 Reduction in free carriers in channel due to –ve potential

In Fig. 4, VGS has been set at a negative voltage such as -1 V. The negative potential at the gate will tend to pressure electrons toward the p-type substrate (like charges repel) and attract holes from the p-type substrate (opposite charges attract) as shown in Fig. 4. Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, the higher the rate of recombination.

For positive values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the p-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 3 reveals that the drain current will increase at a rapid rate.

ENHANCEMENT-TYPE MOSFET

Basic Construction

The basic construction of the n-channel enhancement-type MOSFET is provided in Fig.1. A slab of p-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level.

The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

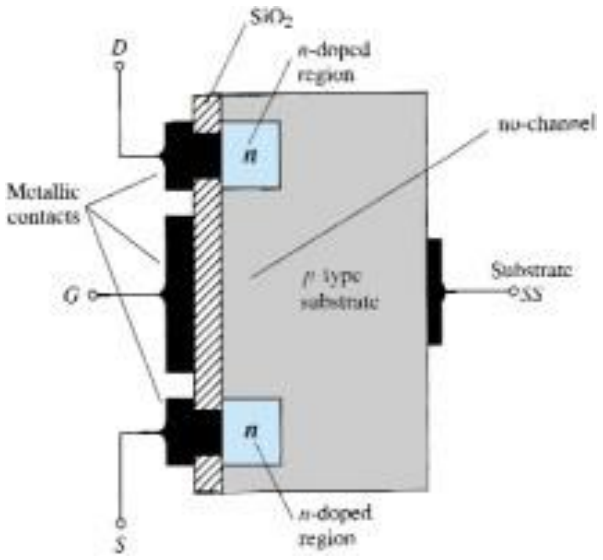


Fig 1. N channel enhancement type MOSFET

Basic Operation and Characteristics

If V_{GS} is set at 0 V and a voltage applied between the drain and source of the device of Fig. 1, the absence of an n-channel (with its generous number of free carriers) will result in a current of effectively zero amperes—quite different from the depletion- type MOSFET and JFET where I_D - I_{DSS}.

It is not sufficient to have a large accumulation of carriers (electrons) at the drain and source (due to the n-doped regions) if a path fails to exist between the two. With VDS some positive voltage, VGS at 0 V, and terminal SS directly connected to the source, there are in fact two reverse-biased p-n junctions between the n-doped regions and the p-substrate to oppose any significant flow between drain and source.

In Fig. 2 both VDS and VGS have been set at some positive voltage greater than 0 V, establishing the drain and gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes (since like charges repel) in the p-substrate along the edge of the SiO2 layer to leave the area and enter deeper regions of the p-substrate, as shown in the figure.

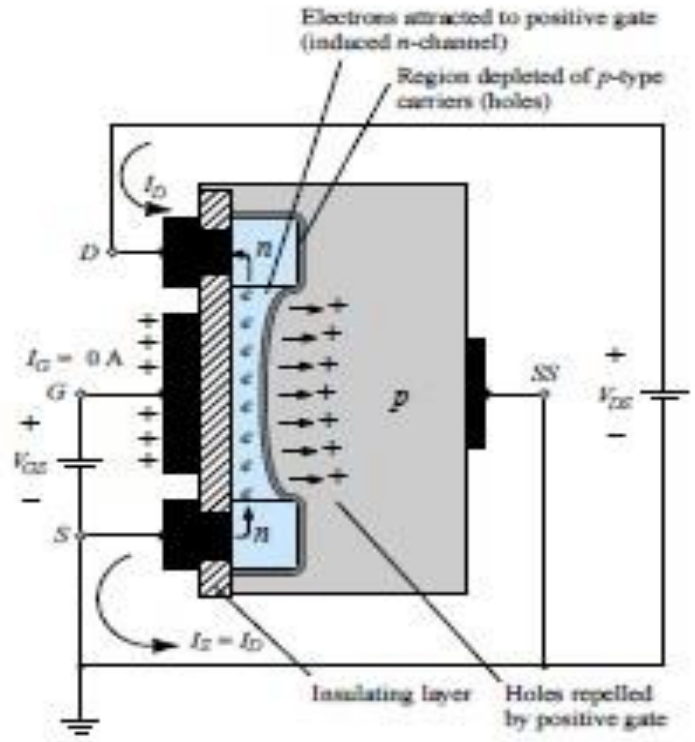


Fig 2. Channel formation

As *VGS* is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold *VGS* constant and increase the level of *VDS*, the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET.

The leveling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 3. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 3, we find that

$$V_{DG} = V_{DS} - V_{GS}$$

The drain characteristics of Fig. 5.34 reveal that for the device of Fig 3 with VGS = 8 V, saturation occurred at a level of VDS = 6 V. In fact, the saturation level for VDS is related to the level of applied VGS by

$$V_{DSsat} = V_{GS} - V_T$$

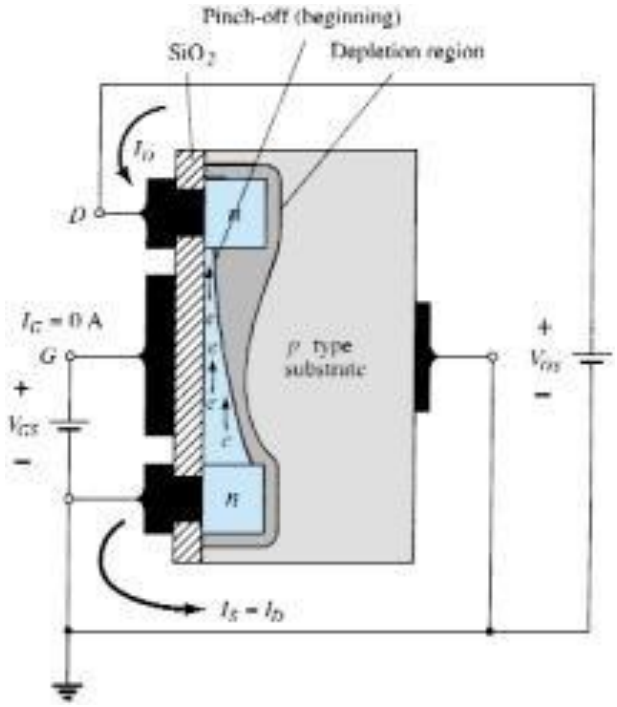


Fig 3. Change in channel and depletion region with increasing V_{DS}

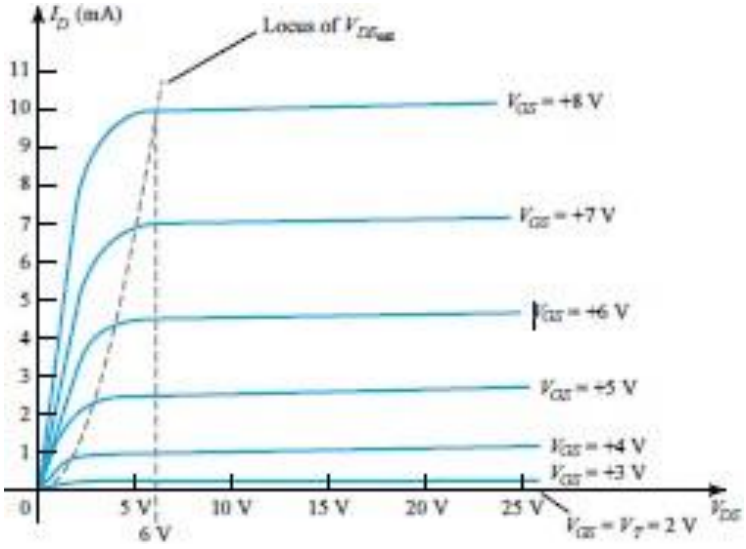


Fig 4. Drain characteristics

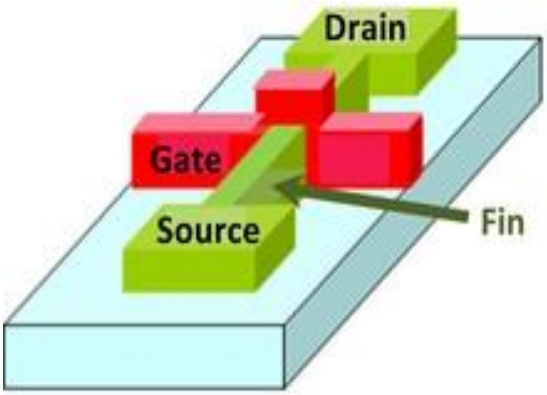
For levels of VGS > VT, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$I_D = k(V_{GS} - V_T)^2$

Again, it is the squared term that results in the nonlinear (curved) relationship between ID and VGS. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation where ID(on) and VGS(on) are the values for each at a particular point on the characteristics of the device.

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

FINFET:



The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the body of the device. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device. In current usage the term FinFET has a less precise definition.

Among microprocessor manufacturers, AMD, IBM, and Motorola describe their double-gate development efforts as FinFET] development whereas Intel avoids using the term to describe their closely related tri-gate architecture. In the technical literature, FinFET is used somewhat generically to describe any fin- based, multigate transistor architecture regardless of number of gates.

A 25-nm transistor operating on just 0.7 volt was demonstrated in December 2002 by Taiwan Semiconductor Manufacturing Company. The "Omega FinFET" design is named after the similarity between the Greek letter omega (Ω) and the shape in which the gate wraps around the source/drain structure. It has a gate delay of just 0.39 picosecond (ps) for the N-type transistor and 0.88 ps for the P-type.

FinFET can also have two electrically independent gates, which gives circuit designers more flexibility to design with efficient, low-power gates.[12]

UNIT IV

SPECIAL SEMICONDUCTOR DEVICES

SCHOTTKY BARRIER (HOT-CARRIER) DIODES

In recent years, there has been increasing interest in a two-terminal device referred to as a Schottky-barrier, surface-barrier, or hot-carrier diode. Its areas of application were first limited to the very high frequency range due to its quick response time (especially important at high frequencies) and a lower noise figure (a quantity of real importance in high-frequency applications). In recent years, however, it is appearing more and more in low-voltage/high-current power supplies and ac-to-dc converters.

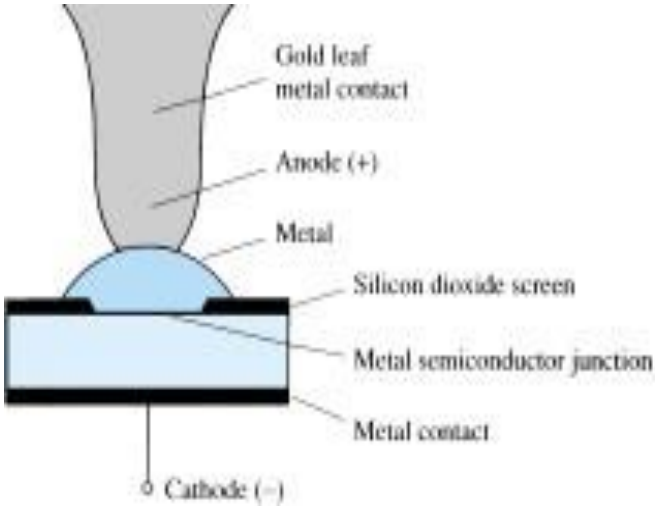


Fig 1. Passivated schottky barrier diode

Its construction is quite different from the conventional p-n junction in that a metalsemiconductor junction is created such as shown in Fig.1. The semiconductor is normally n-type silicon (although p-type silicon is sometimes used), while a host of different metals, such as molybdenum, platinum, chrome, or tungsten, are used. Different construction techniques will result in a different set of characteristics for the device, such as increased frequency range, lower forward bias, and so on. Priorities do not permit an examination of each technique here, but information will usually be provided by the manufacturer. In general, however, Schottky diode construction results in a more uniform junction region and a high level of ruggedness.

In both materials, the electron is the majority carrier. In the metal, the level of minority carriers (holes) is insignificant. When the materials are joined, the electrons in the n-type silicon semiconductor material immediately flow into the adjoining metal, establishing a heavy flow of majority carriers. Since the injected carriers have a very high kinetic energy level compared to the electrons of the metal, they are commonly called –hot carriers.‖

The additional carriers in the metal establish a ―negative wall‖ in the metal at the boundary between the two materials. The net result is a ―surface barrier‖ between the two materials, preventing any further current. That is, any electrons (negatively charged) in the silicon material face a carrier-free region and a ―negative wall‖ at the surface of the metal.

The application of a forward bias as shown in the first quadrant of Fig. 2 will reduce the strength of the negative barrier through the attraction of the applied positive potential for electrons from this region. The result is a return to the heavy flow of electrons across the boundary, the magnitude of which is controlled by the level of the applied bias potential. The barrier at the junction for a Schottky diode is less than that of the p-n junction device in both the forward- and reverse-bias regions. The result is therefore a higher current at the same applied bias in the forward- and reverse-bias regions. This is a desirable effect in the forward-bias region but highly undesirable in the reverse-bias region.

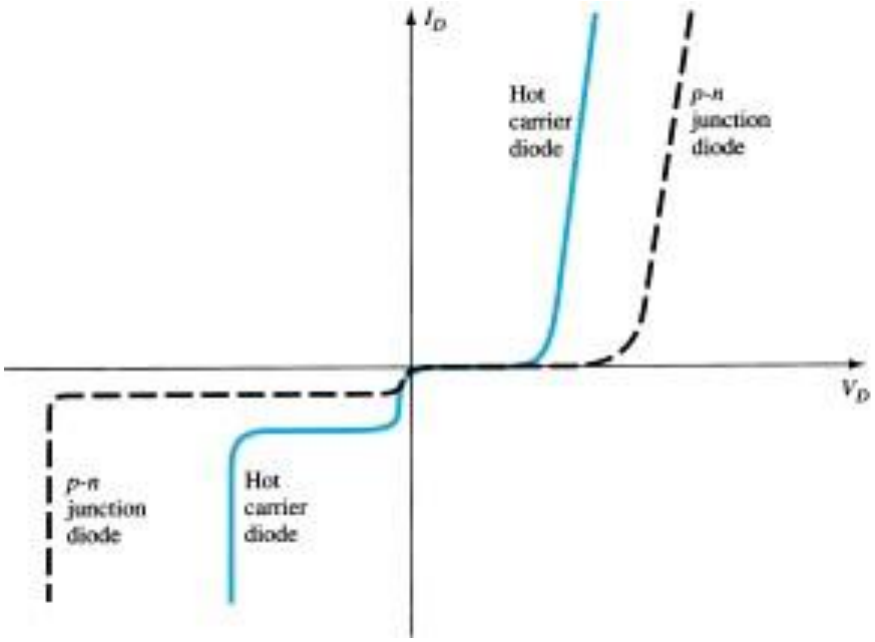


Fig 2. Comparison of characteristics of Hot carrier and pn diode

Applications

- In radar systems,
- Schottky TTL logicfor computers,
- mixers and detectors in communication equipment,
- instrumentation and analog-to-digital converters.

Zener diode

A Zener diode is a type of diode that permits current not only in the forward direction like a normal diode, but also in the reverse direction if the voltage is larger than the breakdown voltage known as "Zener knee voltage" or "Zener voltage". The device was named after Clarence Zener, who discovered this electrical property.

Diode symbol

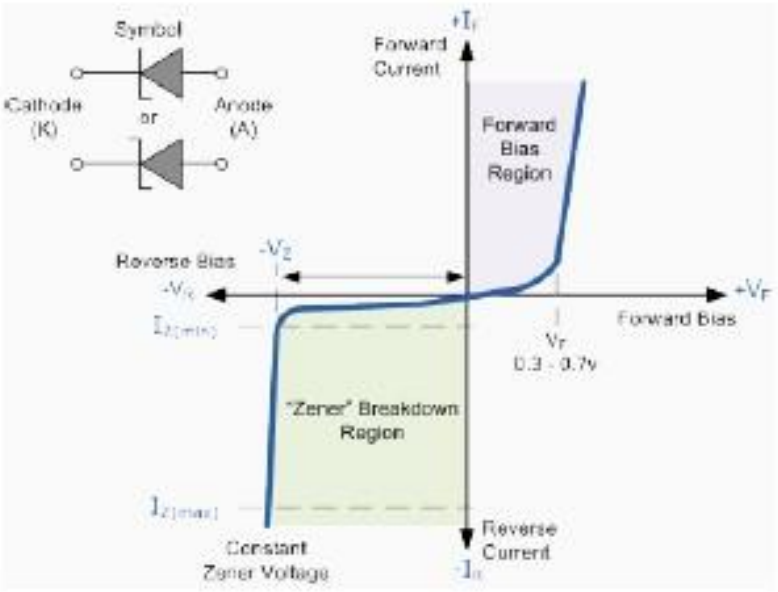
However, the Zener Diode or "Breakdown Diode" as they are sometimes called, are basically the same as the standard PN junction diode but are specially designed to have a low pre-determined Reverse Breakdown Voltage that takes advantage of this high reverse voltage. The point at which a zener diode breaks down or conducts is called the "Zener Voltage" (Vz).

The Zener diode is like a general-purpose signal diode consisting of a silicon PN junction. When biased in the forward direction it behaves just like a normal signal diode passing the rated current, but when a reverse voltage is applied to it the reverse saturation current remains fairly constant over a wide range of voltages. The reverse voltage increases until the diodes breakdown voltage VB is reached at which point a process called Avalanche Breakdown occurs in the depletion layer and the current flowing through the zener diode increases dramatically to the maximum circuit value (which is usually limited by a series resistor). This breakdown voltage point is called the "zener voltage" for zener diodes.

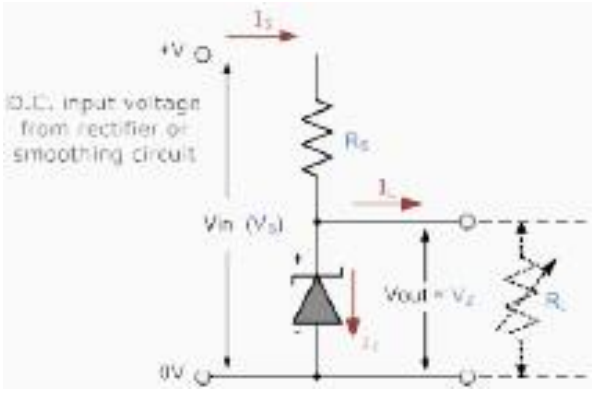
The point at which current flows can be very accurately controlled (to less than 1% tolerance) in the doping stage of the diodes construction giving the diode a specific *zener breakdown voltage*, (Vz) ranging from a few volts up to a few hundred volts. This zener breakdown voltage on the I-V curve is almost a vertical straight line.

Zener diode characteristics

The Zener Diode is used in its "reverse bias" or reverse breakdown mode, i.e. the diodes anode connects to the negative supply. From the I-V characteristics curve above, we can see that the zener diode has a region in its reverse bias characteristics of almost a constant negative voltage regardless of the value of the current flowing through the diode and remains nearly constant even with large changes in current as long as the zener diodes current remains between the breakdown current IZ(min) and the maximum current rating IZ(max).



The Zener Diode Regulator



Zener Diodes can be used to produce a stabilised voltage output with low ripple under varying load current conditions. By passing a small current through the diode from a voltage source, via a suitable current limiting resistor (RS), the zener diode will conduct sufficient current to maintain a voltage drop of Vout. We remember from the previous tutorials that the DC output voltage from the half or full-wave rectifiers contains ripple superimposed onto the DC voltage and that as the load value changes so to does the average output voltage. By connecting a simple zener stabiliser circuit as shown below across the output of the rectifier, a more stable output voltage can be produced**.**

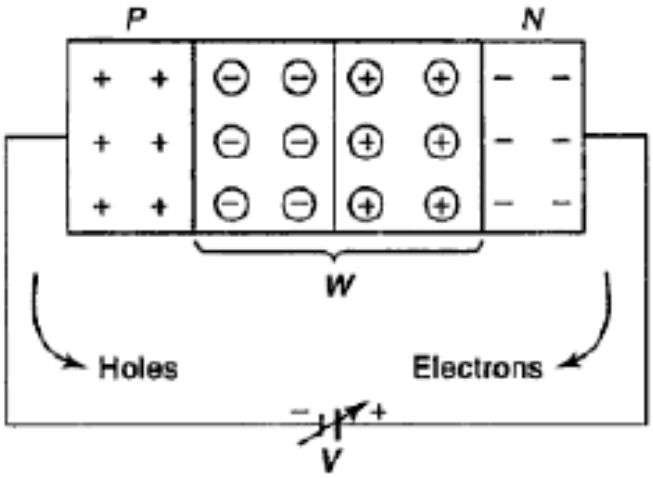
VARACTOR DIODE

A varactor diode is best explained as a variable capacitor. Think of the depletion region as a variable dielectric. The diode is placed in reverse bias. The dielectric is ‑adjusted‖ by reverse bias voltage changes.

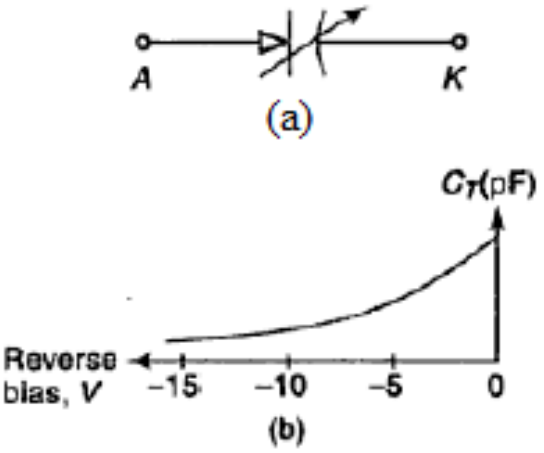
• Junction capacitance is present in all reverse biased diodes because of the depletion region.

• Junction capacitance is optimized in a varactor diode and is used for high frequencies and switching applications.

• Varactor diodes are often used for electronic tuning applications in FM radios and televisions.



Depletion region in a reverse biased PN junction



(a) Circuit symbol of varactor diode (b) Characteristics of varactor diode

• They are also called voltage-variable capacitance diodes.

A Junction diode which acts as a variable capacitor under changing reverse bias is known as VARACTOR DIODE

A varactor diode is specially constructed to have high resistance under reverse bias.

Capacitance for varactor diode are Pico farad. (10-12) range

CT = ЄA / Wd

CT =Total Capacitance of the junction

Є = Permittivity of the semiconductor material
A = Cross sectional area of the junction
WD= Width of the depletion layer

Curve between Reverse bias voltage Vr across varactor diode and total junction capacitance Ct and Ct can be changed by changing Vr.

Tunnel diode(Esaki Diode)

• It was introduced by Leo Esaki in 1958.

• Heavily-doped p-n junction

Impurity concentration is 1 part in 10^3 as compared to 1 part in 10^8 in p-n junction diode

• Width of the depletion layer is very small (about 100 A).

• It is generally made up of Ge and GaAs.

• It shows tunneling phenomenon.

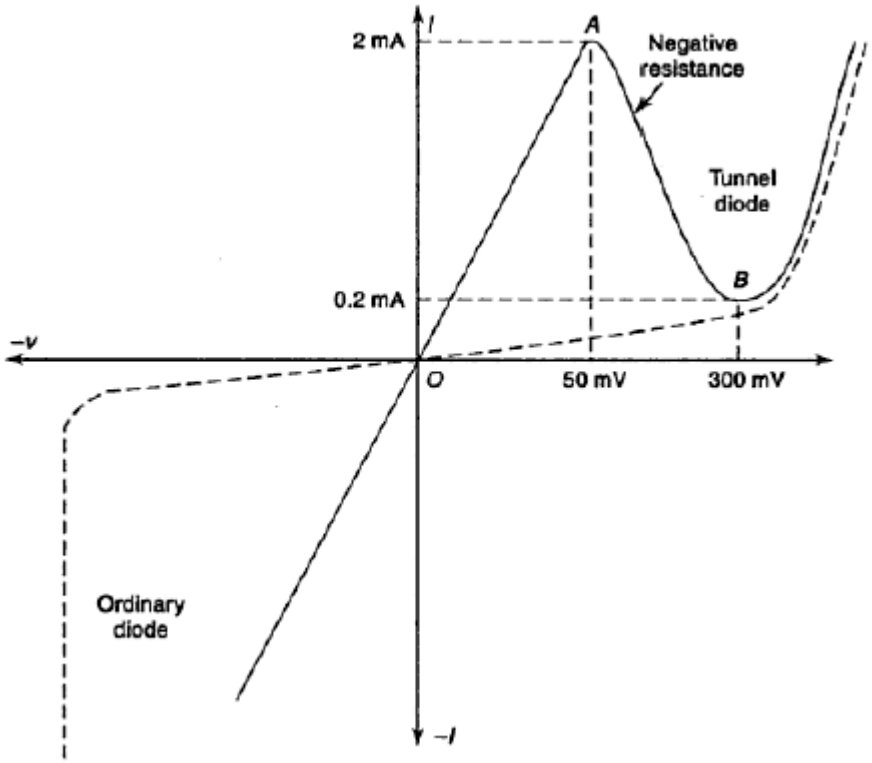
• Circuit symbol of tunnel diode is :

Tunnelling Effect

• Classically, carrier must have energy at least equal to potential-barrier height to cross the junction .

• But according to Quantum mechanics there is finite probability that it can penetrate through the barrier for a thin width.

• This phenomenon is called tunneling and hence the Esaki Diode is known as Tunnel Diode.



V–I characteristic of tunnel diode

ENERGY BAND DIAGRAM

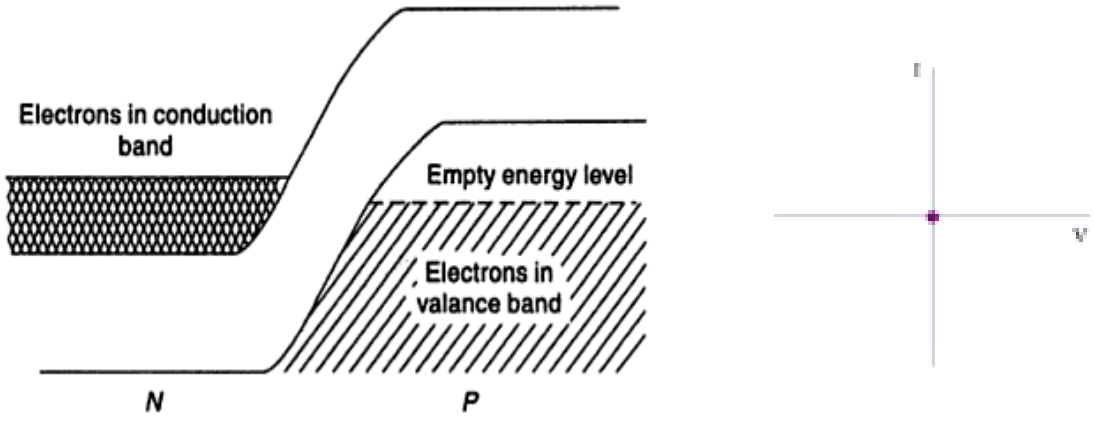
Energy-band diagram of pn junction in thermal equilibrium in which both the n and p region are degenerately doped.

AT ZERO BIAS

Simplified energy-band diagram and I-V characteristics of the tunnel diode at zero bias.

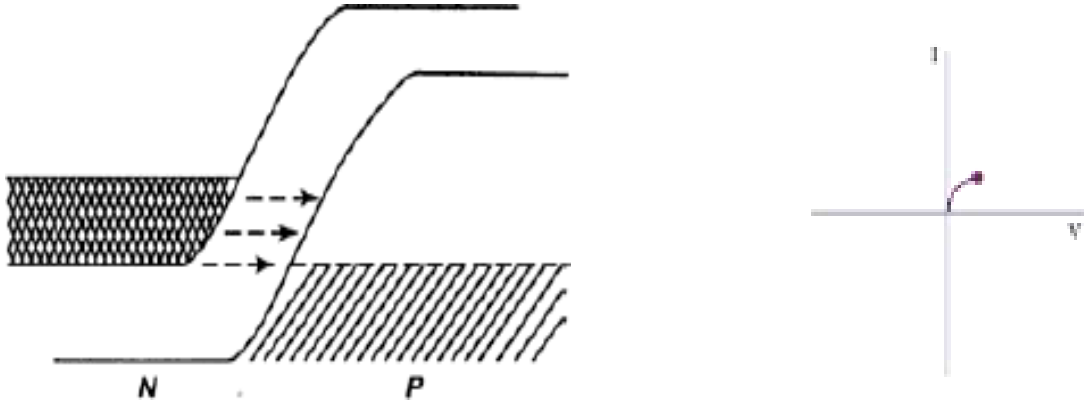
- Zero current on the I-V diagram;

- All energy states are filled below EF on both sides of the junction;



AT SMALL FORWARD VOLTAGE

Simplified energy-band diagram and I-V characteristics of the tunnel diode at a slight forward bias



- Electrons in the conduction band of the n region are directly opposite to the empty states in the valence band of the p region.

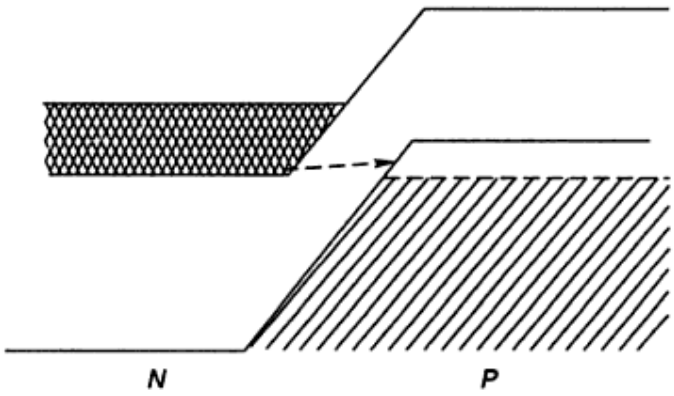
So a finite probability that some electrons tunnel directly into the empty states resulting in forward-bias tunneling current.

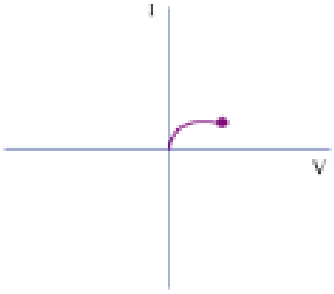
AT MAXIMUM TUNNELING CURENT

Simplified energy-band diagraam and I-V characteristics of the tunnel diode at a forward bias producing maximum tunneling current.

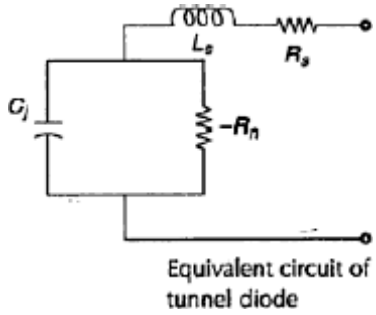
- The maximum number of electrons in the n region are opposite to the maximum number of empty states in the p region.

- Hence tunneling current is maximum.





TUNNEL DIODE EQUIVALENT CIRCUIT



Equivalent circuit of tunnel diode

• This is the equivalent circuit of tunnel diode when biased in negative resistance region.
• At higher frequencies the series R and L can be ignored.
• Hence equivalent circuit can be reduced to parallel combination of junction capacitance and negative resistance.

Applications

- As logic memory storage device
- As microwave oscillator
- In relaxation oscillator circuit
- As an amplifier
- As an ultra-high speed switch

Advantages

- Low noise
- Ease of operation
- High speed
- Low power

Disadvantages

- Voltage range over which it can be operated is 1 V less.
- Being a two terminal device there is no isolation between the input and output circuit.

Laser diode:

A laser diode, or LD, is an electrically pumped semiconductor laser in which the active medium is formed by a p-n junction of a semiconductor diode similar to that found in a light-emitting diode.The laser diode is the most common type of laser produced. Laser diodes have a very wide range of uses that include, but are not limited to, fiber optic communications, barcode readers, laser pointers, CD/DVD/Blu-ray reading, laser printing, scanning and increasingly directional lighting sources.

A laser diode is electrically a P-i-n diode. The active region of the laser diode is in the intrinsic (I) region, and the carriers, electrons and holes, are pumped into it from the N and P regions respectively. While initial diode laser research was conducted on simple P-N diodes, all modern lasers use the double-heterostructure implementation, where the carriers and the photons are confined in order to maximize their chances for recombination and light generation. Unlike a regular diode used in electronics, the goal for a laser diode is that all carriers recombine in the I region, and produce light. Thus, laser diodes are fabricated using direct bandgap semiconductors. The laser diode epitaxial structure is grown using one of the crystal growth techniques, usually starting from an N doped substrate, and growing the I doped active layer, followed by the P doped cladding, and a contact layer. The active layer most often consists of quantum wells, which provide lower threshold current and higher efficiency.

Laser diodes form a subset of the larger classification of semiconductor *p-n* junction diodes. Forward electrical bias across the laser diode causes the two species of charge carrier – holes and electrons – to be "injected" from opposite sides of the *p-n* junction into the depletion region. Holes are injected from the *p*-doped, and electrons from the *n*-doped, semiconductor. (A depletion region, devoid of any charge carriers, forms as a result of the difference in electrical potential between *n*- and *p*-type semiconductors wherever they are in physical contact.) Due to the use of charge injection in powering most diode lasers, this class of lasers is sometimes termed "injection lasers," or "injection laser diode" (ILD). As diode lasers are semiconductor devices, they may also be classified as semiconductor lasers. Either designation distinguishes diode lasers from solid-state lasers.

Another method of powering some diode lasers is the use of optical pumping. Optically pumped semiconductor lasers (OPSL) use a III-V semiconductor chip as the gain medium, and another

laser (often another diode laser) as the pump source. OPSL offer several advantages over ILDs, particularly in wavelength selection and lack of interference from internal electrode structures.[2][3]

When an electron and a hole are present in the same region, they may recombine or "annihilate" with the result being spontaneous emission — i.e., the electron may re-occupy the energy state of the hole, emitting a photon with energy equal to the difference between the electron and hole states involved. (In a conventional semiconductor junction diode, the energy released from the recombination of electrons and holes is carried away as phonons, i.e., lattice vibrations, rather than as photons.) Spontaneous emission gives the laser diode below lasing threshold similar properties to an LED. Spontaneous emission is necessary to initiate laser oscillation, but it is one among several sources of inefficiency once the laser is oscillating.

The difference between the photon-emitting semiconductor laser and conventional phonon-emitting (non-light-emitting) semiconductor junction diodes lies in the use of a different type of semiconductor, one whose physical and atomic structure confers the possibility for photon emission. These photon-emitting semiconductors are the so-called "direct bandgap" semiconductors. The properties of silicon and germanium, which are single-element semiconductors, have bandgaps that do not align in the way needed to allow photon emission and are not considered "direct." Other materials, the so-called compound semiconductors, have virtually identical crystalline structures as silicon or germanium but use alternating arrangements of two different atomic species in a checkerboard-like pattern to break the symmetry. The transition between the materials in the alternating pattern creates the critical "direct bandgap" property. Gallium arsenide, indium phosphide, gallium antimonide, and gallium nitride are all examples of compound semiconductor materials that can be used to create junction diodes that emit light.

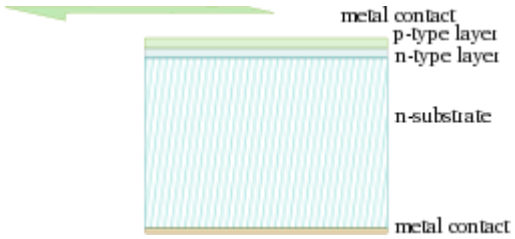


Diagram of a simple laser diode, such as shown above; not to scale

In the absence of stimulated emission (e.g., lasing) conditions, electrons and holes may coexist in proximity to one another, without recombining, for a certain time, termed the "upper-state lifetime" or "recombination time" (about a nanosecond for typical diode laser materials), before they recombine. Then a nearby photon with energy equal to the recombination energy can cause recombination by stimulated emission. This generates another photon of the same frequency, travelling in the same direction, with the same polarization and phase as the first photon. This

means that stimulated emission causes gain in an optical wave (of the correct wavelength) in the injection region, and the gain increases as the number of electrons and holes injected across the junction increases. The spontaneous and stimulated emission processes are vastly more efficient in direct bandgap semiconductors than in indirect bandgap semiconductors; therefore silicon is not a common material for laser diodes.

As in other lasers, the gain region is surrounded with an optical cavity to form a laser. In the simplest form of laser diode, an optical waveguide is made on that crystal surface, such that the light is confined to a relatively narrow line. The two ends of the crystal are cleaved to form perfectly smooth, parallel edges, forming a Fabry–Pérot resonator. Photons emitted into a mode of the waveguide will travel along the waveguide and be reflected several times from each end face before they are emitted. As a light wave passes through the cavity, it is amplified by stimulated emission, but light is also lost due to absorption and by incomplete reflection from the end facets. Finally, if there is more amplification than loss, the diode begins to "lase".

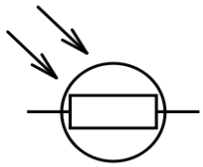
Some important properties of laser diodes are determined by the geometry of the optical cavity. Generally, in the vertical direction, the light is contained in a very thin layer, and the structure supports only a single optical mode in the direction perpendicular to the layers. In the transverse direction, if the waveguide is wide compared to the wavelength of light, then the waveguide can support multiple transverse optical modes, and the laser is known as "multi-mode". These transversely multi-mode lasers are adequate in cases where one needs a very large amount of power, but not a small diffraction-limited beam; for example in printing, activating chemicals, or pumping other types of lasers.

In applications where a small focused beam is needed, the waveguide must be made narrow, on the order of the optical wavelength. This way, only a single transverse mode is supported and one ends up with a diffraction-limited beam. Such single spatial mode devices are used for optical storage, laser pointers, and fiber optics. Note that these lasers may still support multiple longitudinal modes, and thus can lase at multiple wavelengths simultaneously.

The wavelength emitted is a function of the band-gap of the semiconductor and the modes of the optical cavity. In general, the maximum gain will occur for photons with energy slightly above the band-gap energy, and the modes nearest the gain peak will lase most strongly. If the diode is driven strongly enough, additional *side modes* may also lase. Some laser diodes, such as most visible lasers, operate at a single wavelength, but that wavelength is unstable and changes due to fluctuations in current or temperature.

Due to diffraction, the beam diverges (expands) rapidly after leaving the chip, typically at 30 degrees vertically by 10 degrees laterally. A lens must be used in order to form a collimated beam like that produced by a laser pointer. If a circular beam is required, cylindrical lenses and other optics are used. For single spatial mode lasers, using symmetrical lenses, the collimated beam ends up being elliptical in shape, due to the difference in the vertical and lateral divergences. This is easily observable with a red laser pointer.

LDR:



A photoresistor or light-dependent resistor (LDR) or photocell is a resistor whose resistance decreases with increasing incident light intensity; in other words, it exhibits photoconductivity.A photoresistor is made of a high resistance semiconductor. If light falling on the device is of high enough frequency, photons absorbed by the semiconductor give bound electrons enough energy to jump into the conduction band. The resulting free electron (and its hole partner) conduct electricity, thereby lowering resistance.A photoelectric device can be either intrinsic or extrinsic. An intrinsic semiconductor has its own charge carriers and is not an efficient semiconductor, for example, silicon. In intrinsic devices the only available electrons are in the valence band, and hence the photon must have enough energy to excite the electron across the entire bandgap. Extrinsic devices have impurities, also called dopants, added whose ground state energy is closer to the conduction band; since the electrons do not have as far to jump, lower energy photons (that is, longer wavelengths and lower frequencies) are sufficient to trigger the device. If a sample of silicon has some of its atoms replaced by phosphorus atoms (impurities), there will be extra electrons available for conduction.

This is an example of an extrinsic semiconductor. There are many types of photoresistors, with different specifications and models. Photoresistors can be coated with or packaged in different materials that vary the resistance, depending on the use for each LDR.

Applications

Photoresistors come in many types. Inexpensive cadmium sulphide cells can be found in many consumer items such as camera light meters, street lights, clock radios, alarm devices, night lights, outdoor clocks, solar street lamps and solar road studs, etc.They are also used in some dynamic compressors together with a small incandescent lamp or light-emitting diode to control gain reduction.

The use of CdS and CdSe photoresistors is severely restricted in Europe due to the RoHS ban on cadmium.Lead sulphide (PbS) and indium antimonide (InSb) LDRs (light- dependent resistor) are used for the mid-infrared spectral region. Ge:Cu photoconductors are among the best far-infrared detectors available, and are used for infrared astronomy and infrared spectroscopy.

Gallium Arsenide Device:

Gallium arsenide (GaAs) is a compound of the elements gallium and arsenic. It is a III/V semiconductor, and is used in the manufacture of devices such as microwave frequency integrated circuits, monolithic microwave integrated circuits, infrared light-emitting diodes, laser

diodes, solar cells and optical windows.GaAs is often used as a substrate material for the epitaxial growth of other III-V semiconductors including: InGaAs and GaInNAs.

Some electronic properties of gallium arsenide are superior to those of silicon. It has a higher saturated electron velocity and higher electron mobility, allowing gallium arsenide transistors to function at frequencies in excess of 250 GHz. Unlike silicon junctions, GaAs devices are relatively insensitive to heat owing to their wider bandgap. Also, GaAs devices tend to have less noise than silicon devices, especially at high frequencies. This is a result of higher carrier mobilities and lower resistive device parasitics. These properties recommend GaAs circuitry in mobile phones, satellite communications, microwave point-to-point links and higher frequency radar systems. It is used in the manufacture of Gunn diodes for generation of microwaves.

Another advantage of GaAs is that it has a direct band gap, which means that it can be used to emit light efficiently. Silicon has an indirect bandgap and so is very poor at emitting light. Nonetheless, recent advances may make silicon LEDs and lasers possible.

As a wide direct band gap material with resulting resistance to radiation damage, GaAs is an excellent material for space electronics and optical windows in high power applications.

Because of its wide bandgap, pure GaAs is highly resistive. Combined with the high dielectric constant, this property makes GaAs a very good electrical substrate and unlike Si provides natural isolation between devices and circuits. This has made it an ideal material for microwave and millimeter wave integrated circuits, MMICs, where active and essential passive components can readily be produced on a single slice of GaAs.

UNIT V

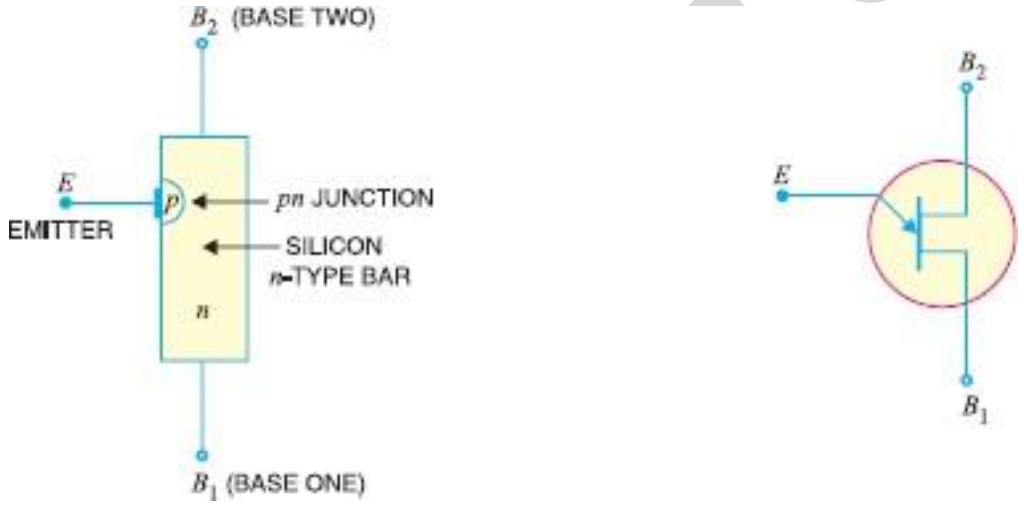
POWER DEVICES AND DISPLAY DEVICES

Uni Junction Transistor (UJT)

A unijunction transistor (UJT) is an electronic semiconductor device that has only one junction.

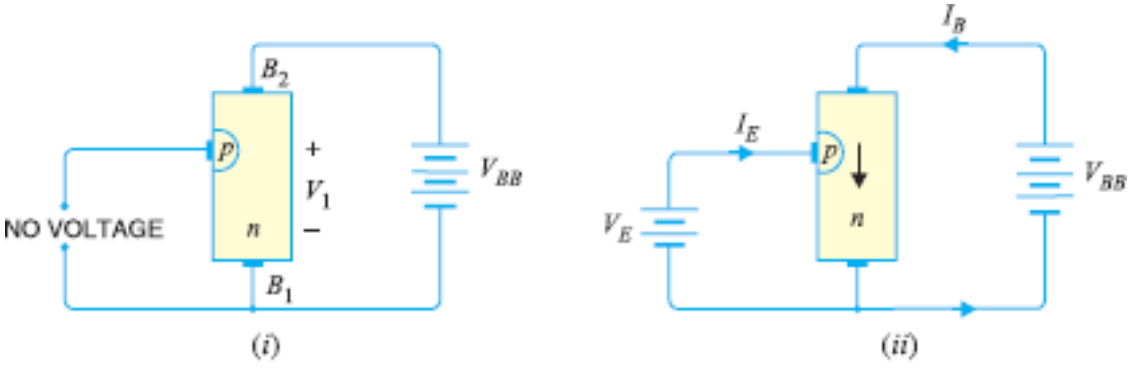
The UJT has three terminals: an emitter (E) and two bases (B1 and B2).

The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is open-circuit is called interbase resistance.



Since the device has one pn junction and three leads it is commonly called UJT.

Operation



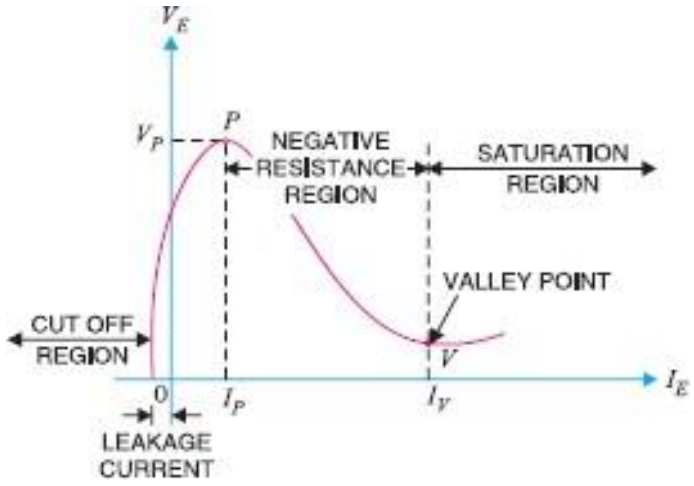
The device has normally B2 is positive w.r.t B1.

(i) If voltage V_{BB} is applied between B2 and B1 with emitter open (fig. i) a voltage gradient is established along the n type bar. The voltage V1 between emitter and B1 establishes a reverse bias of pn junction and the emitter current is cut off. Small leakage current flows from B2 to emitter.

(ii) If a positive voltage is applied at E (fig. ii) the pn junction remains reverse biased as long as the input is less than V1. The voltage exceeds V1 the pn junction become forward biased. Here holes are injected from p type towards B1. The device is ON state.

(iii) If a negative pulse is applied to E, the pn junction is reverse biased and the emitter current is cut off. The device is OFF state.

Characteristics



Initially in the cut off region, as V_E increases from zero, slight leakage current flows from terminalB2 to the emitter.

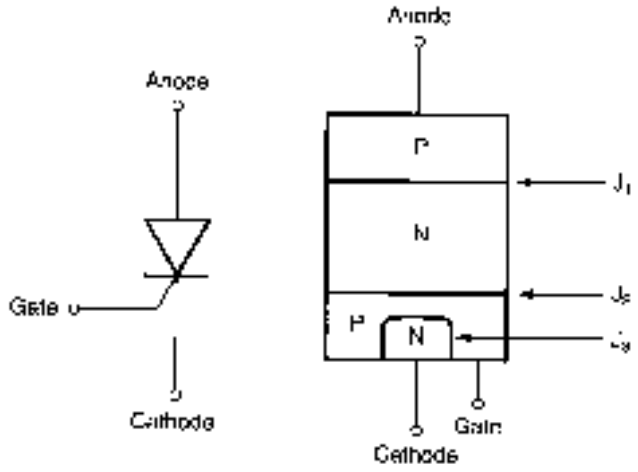
Above a certain value of V_E forward I_E begins to flow, increasing until the peak voltage Vp and current Ip are reached at point P.

After the peak point P an attempt to increase V_E is followed by a sudden increase in emitter current I_E with a corresponding decrease in V_E. This is a negative resistance portion of the curve because in I_E, V_E decreases.

Applications

In switching circuits, Pulse generator and Saw-tooth generator.

Silicon Controlled Rectifier (SCR)



Three terminals

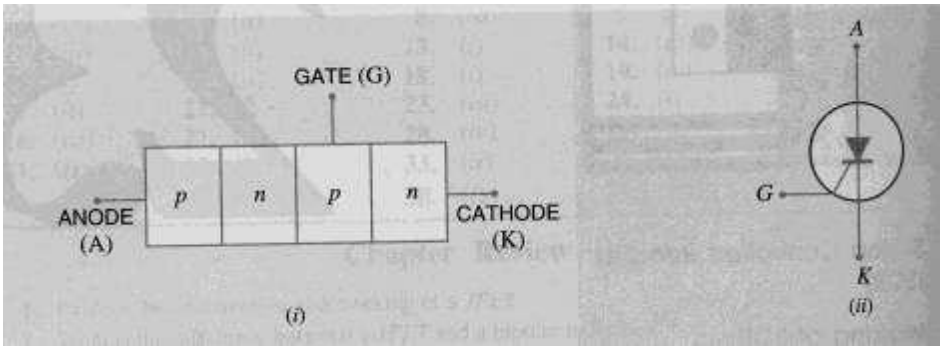
- anode - P-layer
- cathode - N-layer (opposite end)
- gate - P-layer near the cathode

Three junctions - four layers

Connect power such that the anode is positive with respect to the cathode - no current will flow

A silicon controlled rectifier is a semiconductor device that acts as a true electronic switch. It can change alternating current and at the same time can control the amount of power fed to the load. SCR combines the features of a rectifier and a transistor.

CONSTRUCTION



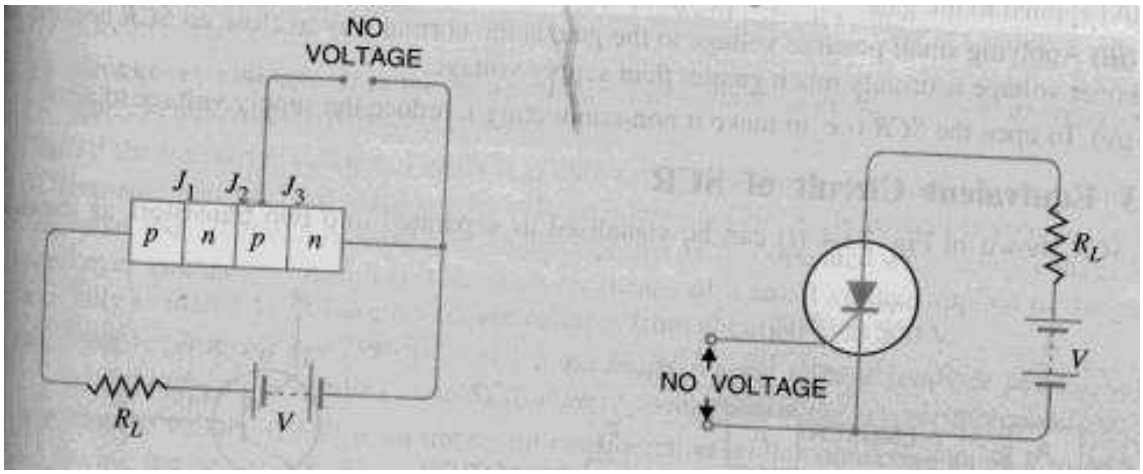
When a pn junction is added to a junction transistor the resulting three pn junction device is called a SCR. ordinary rectifier (pn) and a junction transistor (npn) combined in one unit to form

pnpn device. three terminals are taken : one from the outer p- type material called anode a second from the outer n- type material called cathode K and the third from the base of transistor called Gate. GSCR is a solid state equivalent of thyratron. the gate anode and cathode of SCR correspond to the grid plate and cathode of thyratron SCR is called thyristor.

WORKING PRINCIPLE

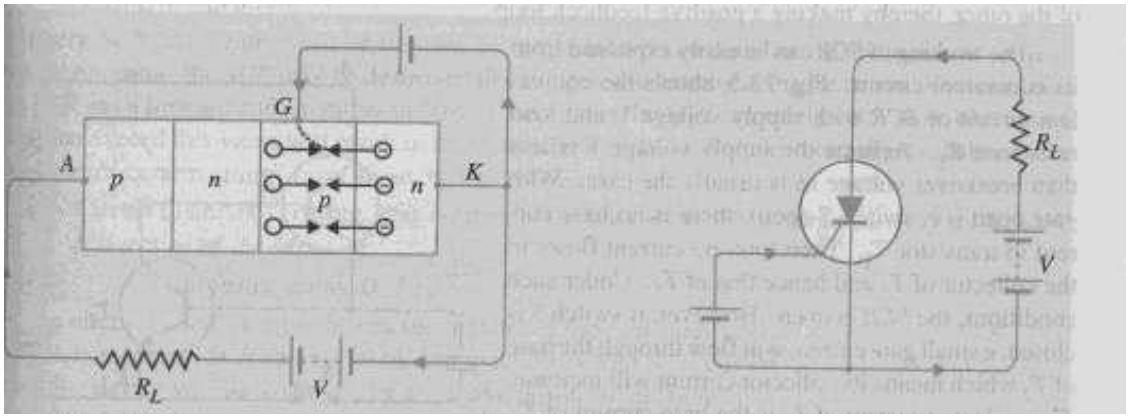
Load is connected in series with anode the anode is always kept at positive potential w.r.t cathode.

WHEN GATE IS OPEN



No voltage applied to the gate, j2 is reverse biased while j1 and j3 are FB . J1 and J3 is just in npn transistor with base open .no current flows through the load RL and SCR is cut off. If the applied voltage is gradually increased a stage is reached when RB junction J2 breakdown .the SCR now conducts heavily and is said to be ON state. the applied voltage at which SCR conducts heavily without gate voltage is called Break over Voltage.

WHEN GATE IS POSITIVE W.R.T CATHODE.



The SCR can be made to conduct heavily at smaller applied voltage by applying small positive potential to the gate.J3 is FB and J2 is RB the electron from n type material start moving across J3 towards left holes from p type toward right. electrons from j3 are attracted across junction J2 and gate current starts flowing. as soon as gate current flows anode current increases. the increased anode current in turn makes more electrons available at J2 breakdown and SCR starts conducting heavily. the gate loses all control if the gate voltage is removed anode current does not decrease at all. The only way to stop conduction is to reduce the applied voltage to zero.

BREAKOVER VOLTAGE

It is the minimum forward voltage gate being open at which SCR starts conducting heavily i.e turned on.

PEAK REVERSE VOLTAGE(PRV)

It is the maximum reverse voltage applied to an SCR without conducting in the reverse direction.

HOLDING CURRENT

It is the maximum anode current gate being open at which SCR is turned off from on conditions.

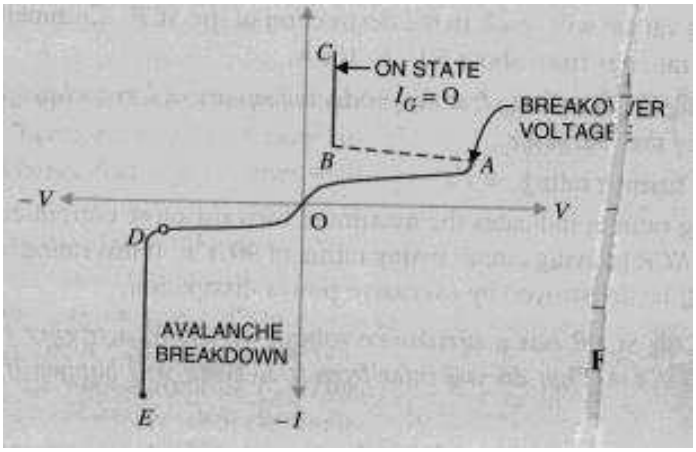
FORWARD CURRENT RATING

It is the maximum anode current that an SCR is capable of passing without destruction

CIRCUIT FUSING RATING

It is the product of of square of forward surge current and the time of duration of the surge.

VI CHARACTERISTICS OF SCR



FORWARD CHARCTERISTICS

When anode is +ve w.r.t cathode the curve between V & I is called Forward characteristics. OABC is the forward characteristics of the SCR at Ig =0. if the supplied voltage is increased from zero point A is reached .SCR starts conducting voltage across SCR suddenly drops (dotted curve AB) most of supply voltage appears across RL

REVERSE CHARCTERISTICS

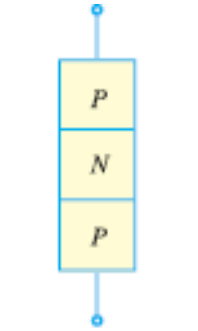
When anode is –ve w.r.t.cathode the curve b/w V&I is known as reverse characteristics reverse voltage come across SCR when it is operated with ac supply reverse voltage is increased anode current remains small avalanche breakdown occurs and SCR starts conducting heavily is known as reverse breakdown voltage

Application

SCR as a switch
SCR Half and Full wave rectifier
SCR as a static contactor
SCR for power control
SCR for speed control of d.c.shunt motor
Over light detector

DIAC (Diode A.C. switch)

A Diac is two terminal , three layer bi directional device which can be switched from its off state for either polarity of applied voltage.



DIAC BASIC CONSTRUCTION


DIAC SYMBOL

Construction

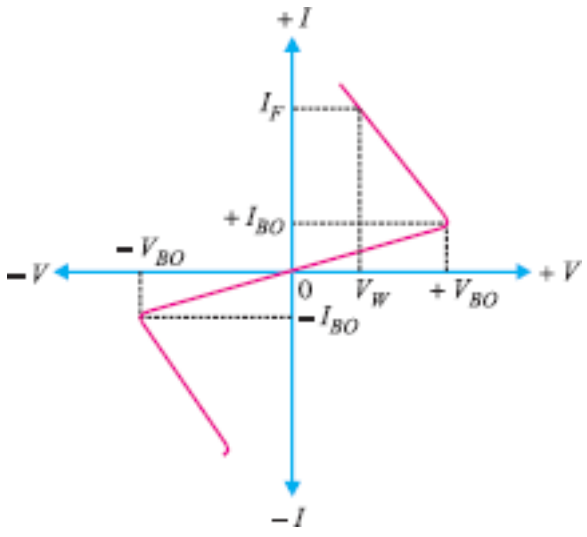
The diac can be constructed in either npn or pnp form.The two leads are connected to p regions of silicon separated by an n region. the structure of diac is similar to that of a transistor differences are

- There is no terminal attached to the base layer
- The three regions are nearly identical in size. the doping concentrations are identical to give the device symmetrical properties.

Operation

When a positive or negative voltage is applied across the terminals of Diac only a small leakage current Ibo will flow through the device as the applied voltage is increased , the leakage current will continue to flow until the voltage reaches breakover voltage Vbo at this point avalanche breakdown of the reverse biased junction occurs and the device exhibits negative resistance i.e current through the device increases with the decreasing values of applied voltage the voltage across the device then drops to breakback voltage Vw.

V- I CHARECTERISTICS OF A DIAC



For applied positive voltage less than + Vbo and Negative voltage less than -Vbo , a small leakage current flows thrugh the device. Under such conditions the diac blocks flow of current and behaves as an open circuit. the voltage +Vbo and -Vbo are the breakdown voltages and usually have range of 30 to 50 volts.

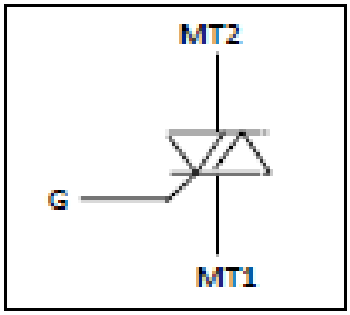
When the positive or negative applied voltage is equal to or greater than tha breakdown voltage Diac begins to conduct and voltage drop across it becomes a few volts conduction then continues until the device current drops below its holding current breakover voltage and holding current values are identical for the forward and reverse regions of operation.

Applications

Diacs are used for triggering of triacs in adjustable phase control of a c mains power. Applications are light dimming heat control universal motor speed control.

TRIAC

Triacs are three terminal devices that are used to switch large a.c. currents with a small trigger signal. Triacs are commonly used in dimmer switches, motor speed control circuits and equipment that automatically controls mains powered equipment including remote control. The triac has many advantages over a relay, which could also be used to control mains equipment; the triac is cheap, it has no moving parts making it reliable and it operates very quickly.

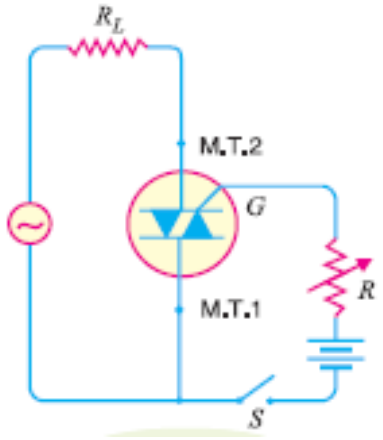


The three terminals on a triac are called Main Terminal 1 (MT1), Main Terminal 2(MT2) and Gate (G). To turn on the triac there needs to be a small current IGT flowing through the gate, this current will only flow when the voltage between G and MT1 is at least VGT. The signal that turns on the triac is called the trigger signal. Once the triac is turned on it will stay on even if there is no gate current until the current flowing between MT2 and MT1 fall below the hold current IH.

Operation

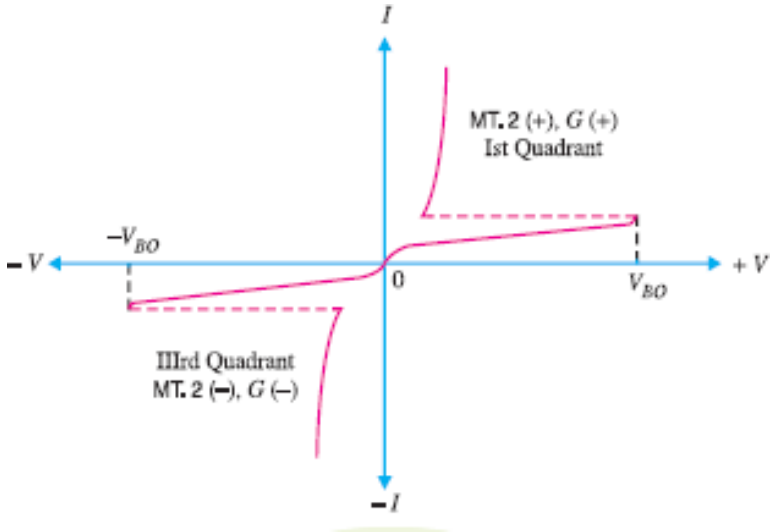
With switch S open, there will be no gate current and the triac is cut off. Even with no current the triac can be turned on provided the supply voltage becomes equal to the breakover voltage.

When switch S is closed, the gate current starts flowing in the gate circuit. Breakover voltage of triac can be varied by making proper currnt flow. Triac starts to conduct wheather MT2 is positive or negative w.r.t MT1.



If terminal MT2 is positive w.r.t MT1 the triac is on and the conventional current will flow from MT2 to MT1.
If terminal MT2 is negative w.r.t MT1 the triac is again turned on and the conventional current will flow from MT1 to MT2.

Characteristics



The V-I curve for triac in the Ist and IIIrd quadrants are essentially identical to SCR in the Ist quadrant.

The triac can be operated with either positive or negative gate control voltage but in normal operation usually the gate voltage is positive in quadrant I and negative in quadrant III.

The supply voltage at which the triac is ON depends upon gate current. The greater gate current and smaller supply voltage at which triac is turned on. This permits to use triac to control a,c. power in a load from zero to full power in a smooth and continuous manner with no loss in the controlling device.

VMOS

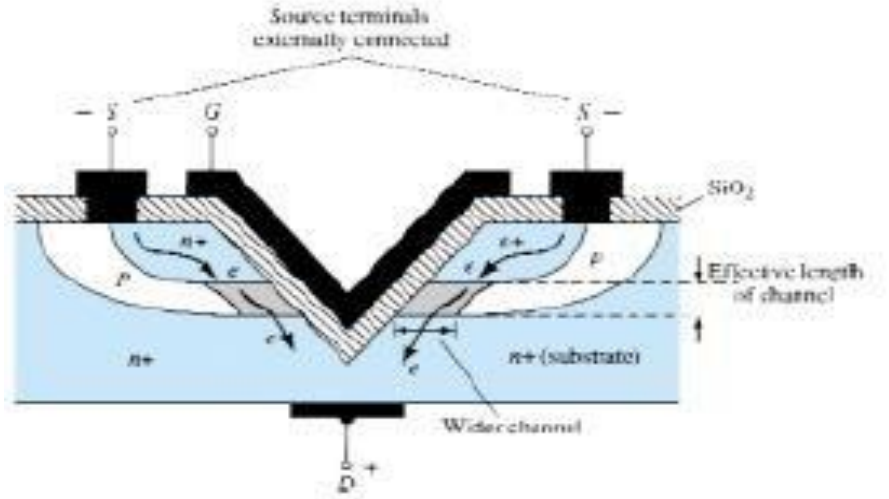
One of the disadvantages of the typical MOSFET is the reduced power-handling levels (typically, less than 1 W) compared to BJT transistors. This shortfall for a device with so many positive characteristics can be softened by changing the construction mode from one of a planar nature to one with a vertical structure as shown in Fig.

All the elements of the planar MOSFET are present in the vertical metal-oxide-silicon FET (VMOS)—the metallic surface connection to the terminals of the device—the SiO2 layer between the gate and the p-type region between the drain and source for the growth of the induced n-channel (enhancement- mode operation). The term vertical is due primarily to the fact that the channel is now formed in the vertical direction rather than the horizontal direction for the planar device.

However, the channel of Fig. also has the appearance of a –V‖ cut in the semiconductor base, which often stands out as a characteristic for mental memorization of the name of the device. The construction of Fig is somewhat simplistic in nature, leaving out some of the transition levels of doping, but it does permit a description of the most important facets of its operation.

The application of a positive voltage to the drain and a negative voltage to the source with the gate at 0 V or some typical positive –on‖ level as shown in Fig. will result in the induced n-channel in the narrow p-type region of the device. The length of the channel is now defined by the vertical height of the p-region, which can be made significantly less than that of a channel using planar construction. On a horizontal plane the length of the channel is limited to 1 to 2 μm.

Diffusion layers can be controlled to small fractions of a micrometer. Since decreasing channel lengths result in reduced resistance levels, the power dissipation level of the device (power lost in the form of heat) at operating current levels will be reduced. In addition, the contact area between the channel and the no region is greatly increased by the vertical mode construction, contributing to a further decrease in the resistance level and an increased area for current between the doping layers.



VMOS construction.

There is also the existence of two conduction paths between drain and source, as shown in Fig., to further contribute to a higher current rating. The net result is a device with drain currents that can reach the ampere levels with power levels exceeding 10 W.

Compared with commercially available planar MOSFETs, VMOS FETs have reduced channel resistance levels and higher current and power ratings.

VMOS FETs have a positive temperature coefficient that will combat the possibility of thermal runaway.

The reduced charge storage levels result in faster switching times for VMOS construction compared to those for conventional planar construction**.**

In fact, VMOS devices typically have switching times less than one-half that encountered for the typical BJT transistor.

LIQUID-CRYSTAL DISPLAYS

The liquid-crystal display (LCD) has the distinct advantage of having a lower power requirement than the LED. It is typically in the order of microwatts for the display, as compared to the same order of milliwatts for LEDs. It does, however, require an external or internal light source and is limited to a temperature range of about 0° to 60°C. Lifetime is an area of concern because LCDs can chemically degrade. The types receiving the major interest today are the field-effect and dynamic-scattering units.

A liquid crystal is a material (normally organic for LCDs) that will flow like a liquid but whose molecular structure has some properties normally associated with solids. For the light-

scattering units, the greatest interest is in the nematic liquid crystal, having the crystal structure shown in Fig 1.

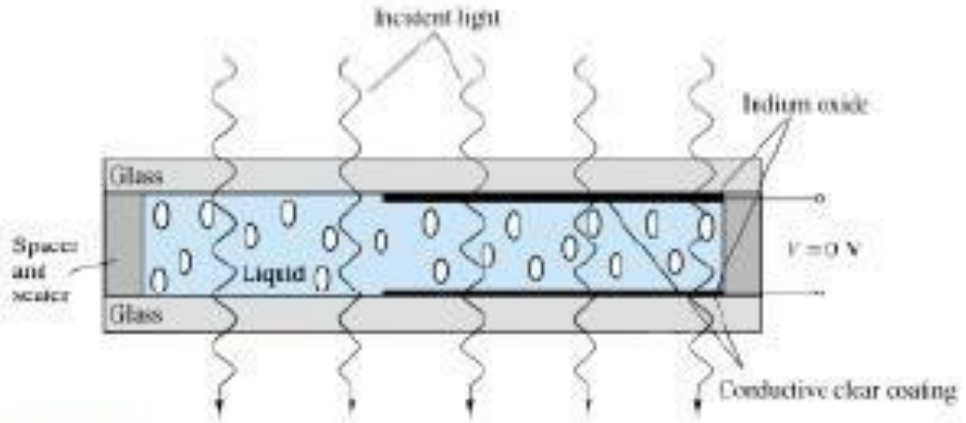


Figure 1 Nematic liquid crystal with no applied bias.

The individual molecules have a rodlike appearance as shown in the figure. The indium oxide conducting surface is transparent, and under the condition shown in the figure, the incident light will simply pass through and the liquid-crystal structure will appear clear. If a voltage (for commercial units the threshold level is usually between 6 and 20 V) is applied across the conducting surfaces, as shown in Fig. 2, the molecular arrangement is disturbed, with the result that regions will be established with different indices of refraction.

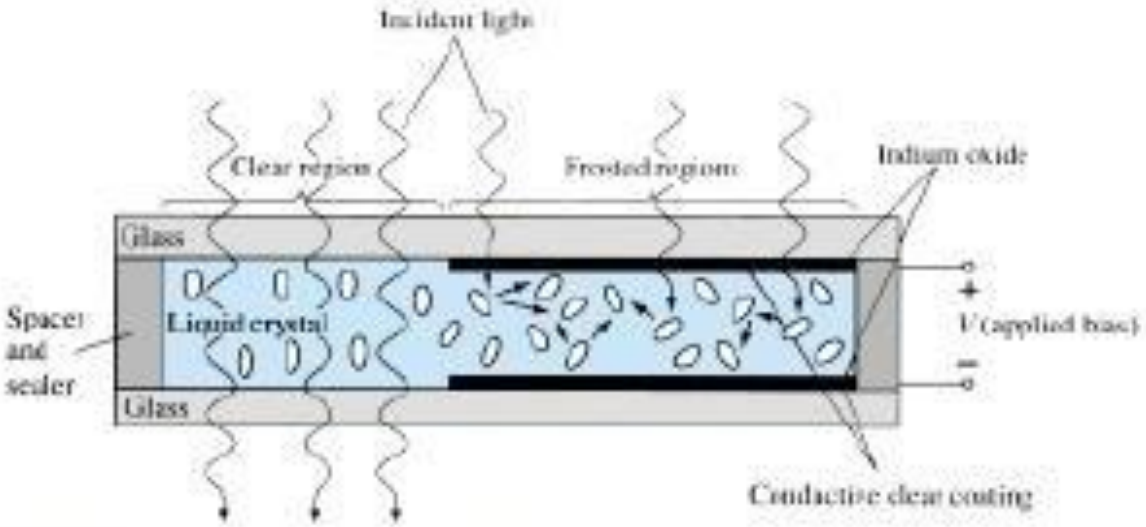


Figure 2 Nematic liquid crystal with applied bias.

A digit on an LCD display may have the segment appearance shown in Fig. 3. The black area is actually a clear conducting surface connected to the terminals below for external control. Two similar masks are placed on opposite sides of a sealed thick layer of liquid-crystal material. If the number 2 were required, the terminals 8, 7, 3, 4, and 5 would be energized, and only those regions would be frosted while the other areas would remain clear.

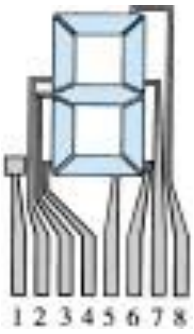


Figure 3. LCD 8 segment digit display

The field-effect or twisted nematic LCD has the same segment appearance and thin layer of encapsulated liquid crystal, but its mode of operation is very different. Similar to the dynamic-scattering LCD, the field-effect LCD can be operated in the reflective or transmissive mode with an internal source. The transmissive display appears in Fig. 4. The internal light source is on the right, and the viewer is on the left. This figure is most noticeably different from Fig. 20.35 in that there is an addition of a light polarizer. Only the vertical component of the entering light on the right can pass through the vertical-light polarizer on the right.

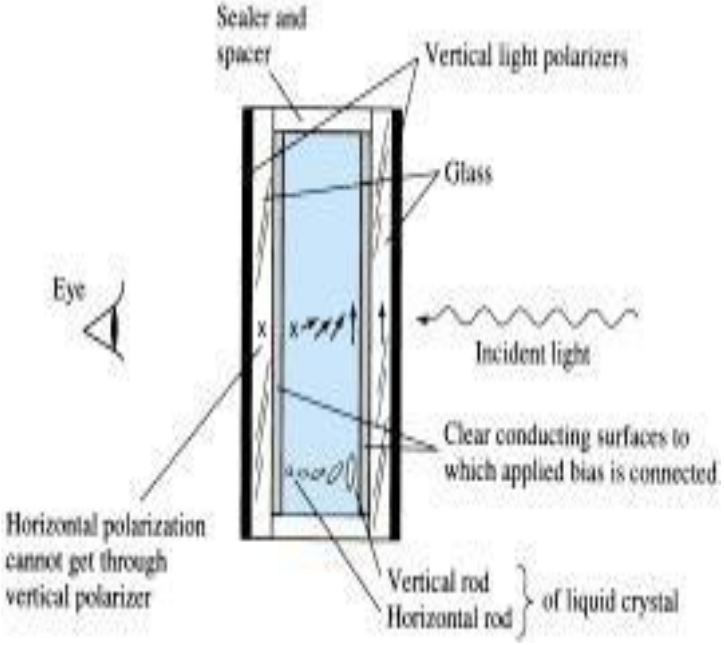


Figure 4. Transmissive field effect LCD with no applied bias

The reflective-type field-effect LCD is shown in Fig. 5. In this case, the horizontally polarized light at the far left encounters a horizontally polarized filter and passes through to the reflector, where it is reflected back into the liquid crystal, bent back to the other vertical polarization, and returned to the observer. If there is no applied voltage, there is a uniformly lit display. The application of a voltage results in a vertically incident light encountering a horizontally polarized filter at the left, which it will not be able to pass through and will be reflected.

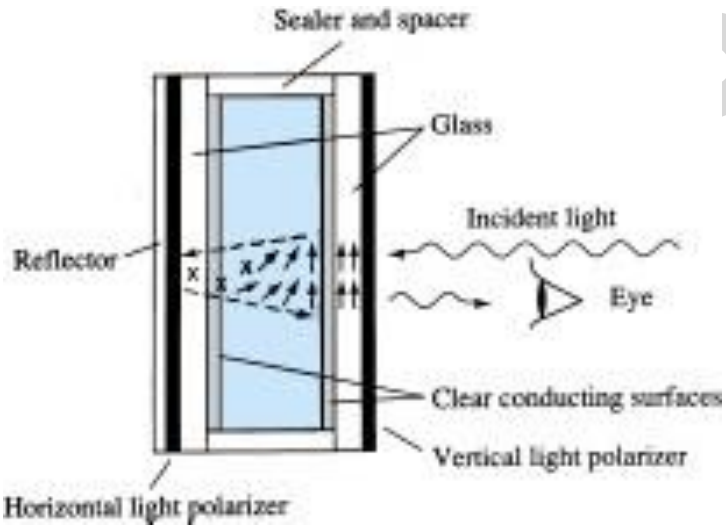


Figure 5. Reflective field effect LCD with no applied bias

Advantages of LCD

- Low power is required
- Good contrast
- Low cost

Disadvantages of LCD

- Speed of operation is slow
- LCD occupy a large area
- LCD life span is quite small, when used on d.c. Therefore, they are used with a.c. suppliers.

Applications of LCD

- Used as numerical counters for counting production items.
- Analog quantities can also be displayed as a number on a suitable device. (e.g.) Digital multimeter.
- Used for solid state video displays.

- Used for image sensing circuits.
- Used for numerical display in pocket calculators.

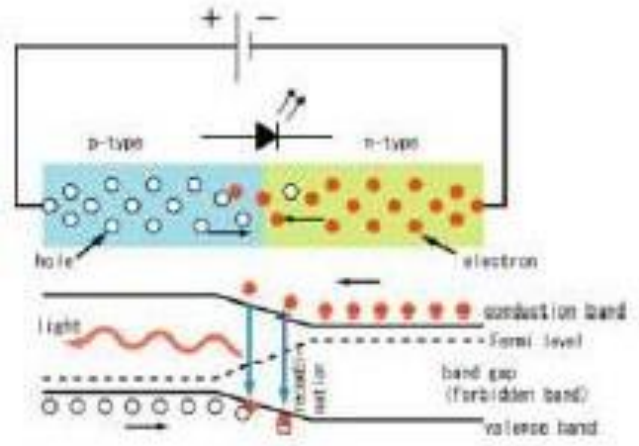
LIGHT EMITTING DIODE (LED)

A light-emitting diode (LED) is a semiconductor light source. LEDs are used as indicator lamps in many devices, and are increasingly used for lighting. Introduced as a practical electronic component in 1962, early LEDs emitted low-intensity red light, but modern versions are available across the visible, ultraviolet and infrared wavelengths, with very high brightness.

When a light-emitting diode is forward biased (switched on), electrons are able to recombine with electron holes within the device, releasing energy in the form of photons. This effect is called electroluminescence and the color of the light (corresponding to the energy of the photon) is determined by the energy gap of the semiconductor. An LED is often small in area (less than 1 mm2), and integrated optical components may be used to shape its radiation pattern.[3] LEDs present many advantages over incandescent light sources including lower energy consumption, longer lifetime, improved robustness, smaller size, faster switching, and greater durability and reliability. LEDs powerful enough for room lighting are relatively expensive and require more precise current and heat management than compact fluorescent lamp sources of comparable output.

Light-emitting diodes are used in applications as diverse as replacements for aviation lighting, automotive lighting (particularly brake lamps, turn signals and indicators) as well as in traffic signals. The compact size, the possibility of narrow bandwidth, switching speed, and extreme reliability of LEDs has allowed new text and video displays and sensors to be developed, while their high switching rates are also useful in advanced communications technology. Infrared LEDs are also used in the remote control units of many commercial products including televisions, DVD players, and other domestic appliances.

SYMBOL OF LED



DIODE I-V CURVE

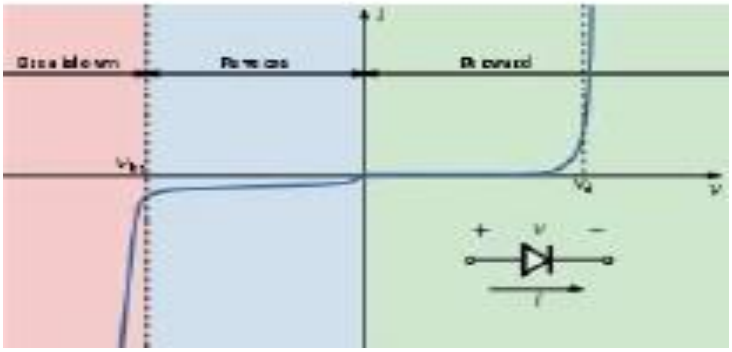


PHOTO TRANSISTORS

Phototransistor, has a photosensitive collector–base p-n junction. The current induced by photoelectric effects is the base current of the transistor. If we assign the notation I for the photoinduced base current, the resulting collector current, on an approximate basis, is

$$I_C = h_{fe} I_\lambda$$

A representative set of characteristics for a phototransistor is provided in Fig. with the symbolic representation of the device. Note the similarities between these curves and those of a typical bipolar transistor.

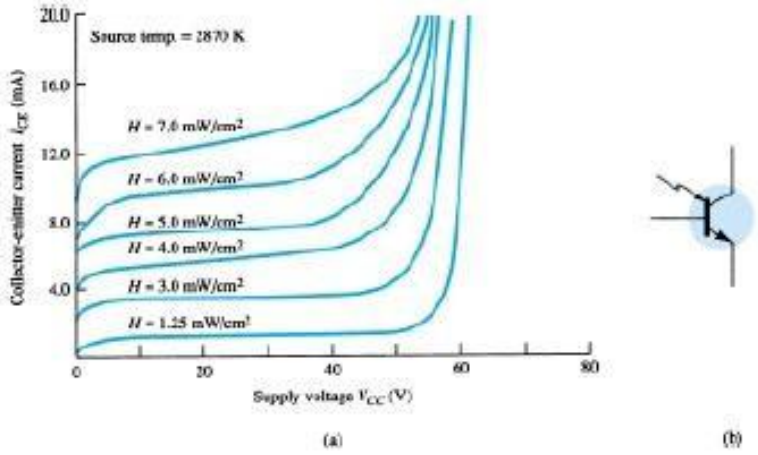
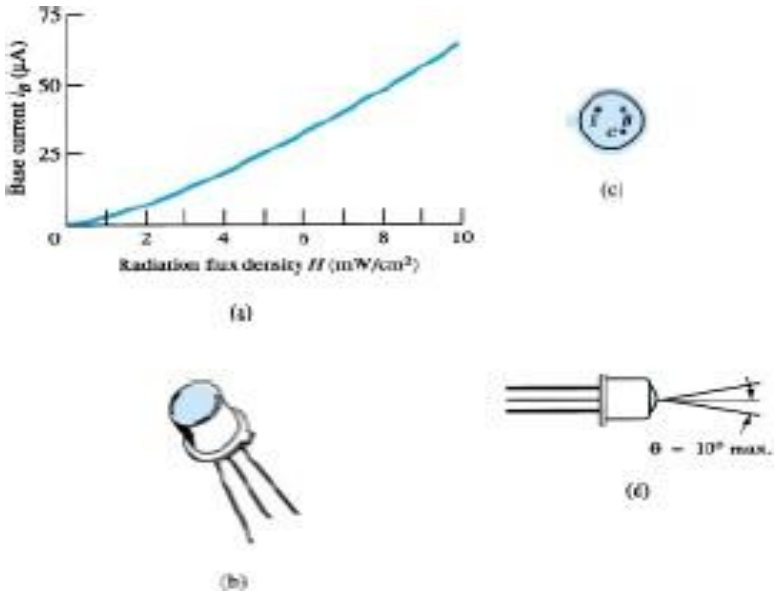


Photo Transistor (a) collector characteristics (b) symbol

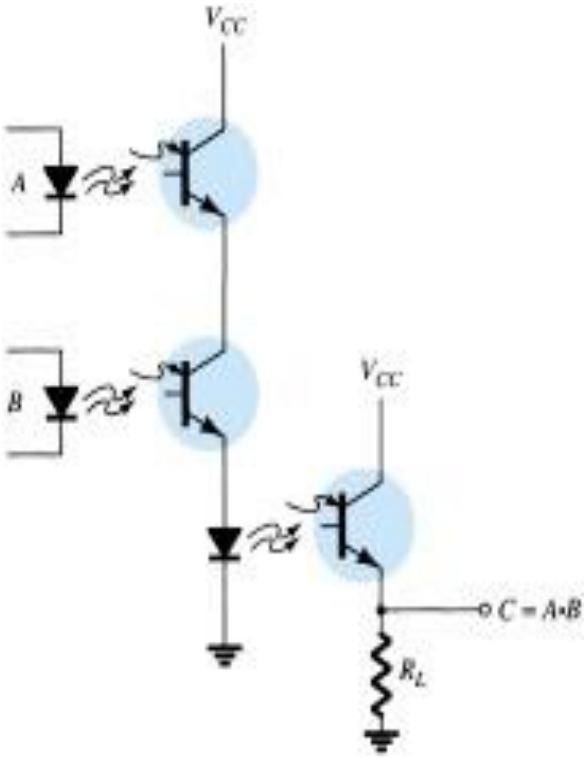


Phototransistor (a) base current vs flux density (b) Device
(c) Terminal identification (d) angular alignment

A high-isolation AND gate is shown in Fig using three phototransistors and three LEDs (light-emitting diodes). The LEDs are semiconductor devices that emit light at an intensity

determined by the forward current through the device. The terminology high isolation simply refers to the lack of an electrical connection between the input and output circuits.

High isolation AND gate employing phototransistor and LED



Applications

Some of the areas of application for the phototransistor include punch-card readers, computer logic circuitry, lighting control (highways, etc.), level indication, relays, and counting systems.

SOLAR CELLS

In recent years, there has been increasing interest in the solar cell as an alternative source of energy. When we consider that the power density received from the sun at sea level is about 100 mW/cm^2 (1 kW/m2), it is certainly an energy source that requires further research and development to maximize the conversion efficiency from solar to electrical energy.

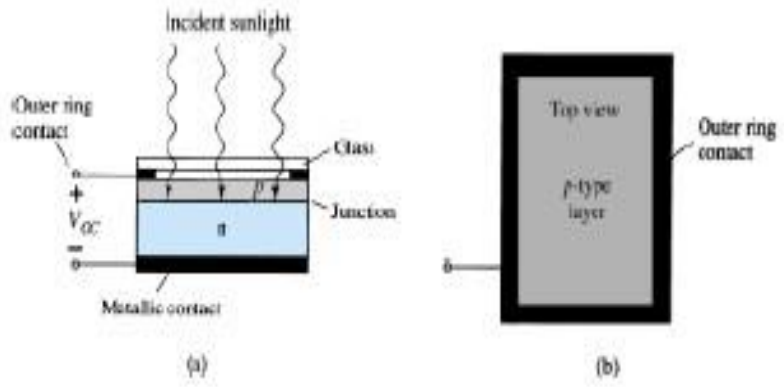


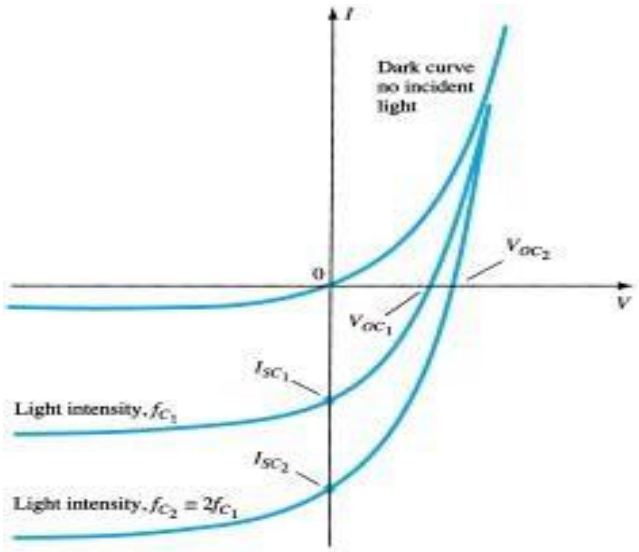
Fig 1. (a) cross section; (b) top view

The basic construction of a silicon p-n junction solar cell appears in Fig. 1. As shown in the top view, every effort is made to ensure that the surface area perpendicular to the sun is a maximum. Also, note that the metallic conductor connected to the p-type material and the thickness of the p-type material are such that they ensure that a maximum number of photons of light energy will reach the junction. A photon of light energy in this region may collide with a valence electron and impart to it sufficient energy to leave the parent atom. The result is a generation of free electrons and holes. This phenomenon will occur on each side of the junction.

In the p-type material, the newly generated electrons are minority carriers and will move rather freely across the junction as explained for the basic p-n junction with no applied bias. A similar discussion is true for the holes generated in the n-type material. The result is an increase in the minority-carrier flow, which is opposite in direction to the conventional forward current of a p-n junction. This increase in reverse current is shown in Fig. 2. Since V= 0 anywhere on the vertical axis and represents a short-circuit condition, the current at this intersection is called the short-circuit current and is represented by the notation I_{SC}.

Under open-circuit conditions (id = 0), the photovoltaic voltage V_{OC} will result. This is a logarithmic function of the illumination, as shown in Fig. 3. V_{OC} is the terminal voltage of a battery under no-load (open-circuit) conditions. Note, however, in the same figure that the short-circuit current is a linear function of the illumination. That is, it will double for the same increase in illumination (f_{C1} and $2f_{C1}$ in Fig. 3) while the change in V_{OC} is less for this region. The major increase in V_{OC} occurs for lower-level increases in illumination. Eventually, a further increase in illumination will have very little effect on V_{OC}, although I_{SC} will increase, causing the power capabilities to increase.

Selenium and silicon are the most widely used materials for solar cells, although gallium arsenide, indium arsenide, and cadmium sulfide, among others, are also used.



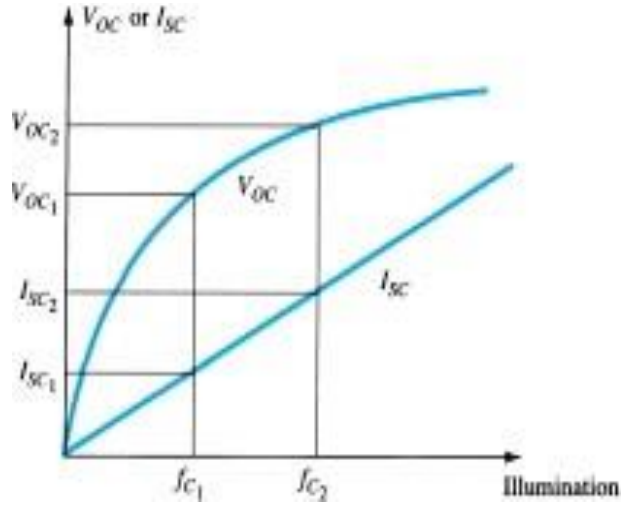


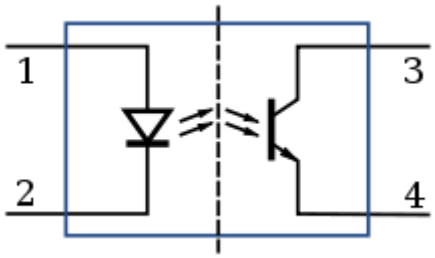
Fig 2. V-I curve for solar cell

Fig 3. Voc and Isc versus illumination for solar cell

OPTO COUPLER:

In electronics, an opto-isolator, also called an optocoupler, photocoupler, or optical isolator, is a component that transfers electrical signals between two isolated circuits by using light. Opto-isolators prevent high voltages from affecting the system receiving the signal. Commercially available opto-isolators withstand input-to-output voltages up to 10 kV and voltage transients with speeds up to 10 kV/μs. A common type of opto-isolator consists of an LED and a

phototransistor in the same package. Opto-isolators are usually used for transmission of digital (on/off) signals, but some techniques allow use with analog (proportional) signals.



An opto-isolator contains a source (emitter) of light, almost always a near infrared light-emitting diode (LED), that converts electrical input signal into light, a closed optical channel (also called dielectrical channel), and a photosensor, which detects incoming light and either generates electric energy directly, or modulates electric current flowing from an external power supply. The sensor can be a photoresistor, a photodiode, a phototransistor, a silicon-controlled rectifier (SCR) or a triac. Because LEDs can sense light in addition to emitting it, construction of symmetrical, bidirectional opto-isolators is possible. An optocoupled solid state relay contains a photodiode opto-isolator which drives a power switch, usually a complementary pair of MOSFETs. A slotted optical switch contains a source of light and a sensor, but its optical channel is open, allowing modulation of light by external objects obstructing the path of light or reflecting light into the sensor.

CCD:

A charge-coupled device (CCD) is a device for the movement of electrical charge, usually from within the device to an area where the charge can be manipulated, for example conversion into a digital value. This is achieved by "shifting" the signals between stages within the device one at a time. CCDs move charge between capacitive *bins* in the device, with the shift allowing for the transfer of charge between bins. The CCD is a major piece of technology in digital imaging. In a CCD image sensor, pixels are represented by p-doped MOS capacitors. These capacitors are biased above the threshold for inversion when image acquisition begins, allowing the conversion of incoming photons into electron charges at the semiconductor-oxide interface; the CCD is then used to read out these charges. Although CCDs are not the only technology to allow for light detection, CCD image sensors are widely used in professional, medical, and scientific applications where high-quality image data is required. In applications with less exacting quality demands, such as consumer and professional digital cameras, active pixel sensors (CMOS) are generally used; the large quality advantage CCDs enjoyed early on has narrowed over time.

In a CCD for capturing images, there is a photoactive region (an epitaxial layer of silicon), and a transmission region made out of a shift register (the CCD, properly speaking).An image is projected through a lens onto the capacitor array (the photoactive region), causing each capacitor to accumulate an electric charge proportional to the light intensity at that location. A one-dimensional array, used in line-scan cameras, captures a single slice of the image, while a two-dimensional array, used in video and still cameras, captures a two-dimensional picture corresponding to the scene projected onto the focal plane of the sensor. Once the array has been

exposed to the image, a control circuit causes each capacitor to transfer its contents to its neighbor (operating as a shift register). The last capacitor in the array dumps its charge into a charge amplifier, which converts the charge into a voltage. By repeating this process, the controlling circuit converts the entire contents of the array in the semiconductor to a sequence of voltages. In a digital device, these voltages are then sampled, digitized, and usually stored in memory; in an analog device (such as an analog video camera), they are processed into a continuous analog signal (e.g. by feeding the output of the charge amplifier into a low-pass filter) which is then processed and fed out to other circuits for transmission, recording, or other processing.